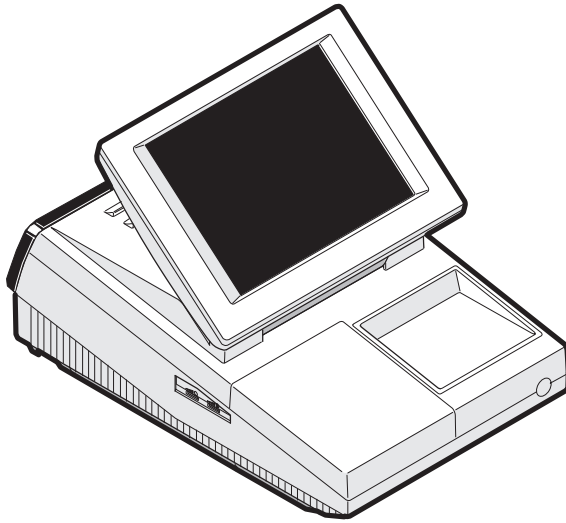


SHARP SERVICE MANUAL

CODE: 00ZUP3300USME



POS TERMINAL

MODEL UP-3300

(For "U" & "A" version)

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PARTS GUIDE	

Parts marked with "⚠" is important for maintaining the safety of the set. Be sure to replace these parts with specified ones for maintaining the safety and performance of the set.

SHARP CORPORATION

This document has been published to be used
for after sales service only.
The contents are subject to change without notice.

BATTERY DISPOSAL

Contains Nickel Metal Hydride Battery. Must be Disposed of Properly.

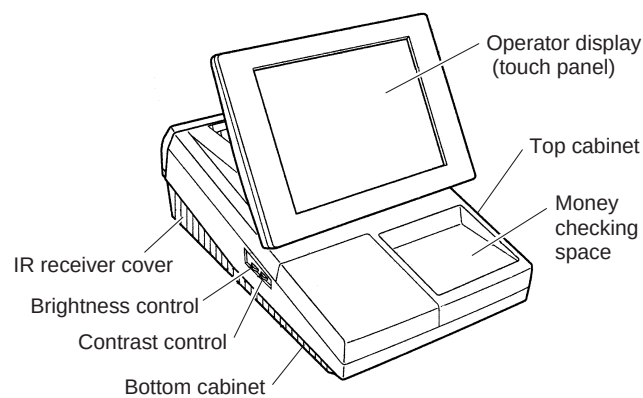
Contact Local Environmental Officials for Disposal Instructions.

CHAPTER 1. SPECIFICATIONS

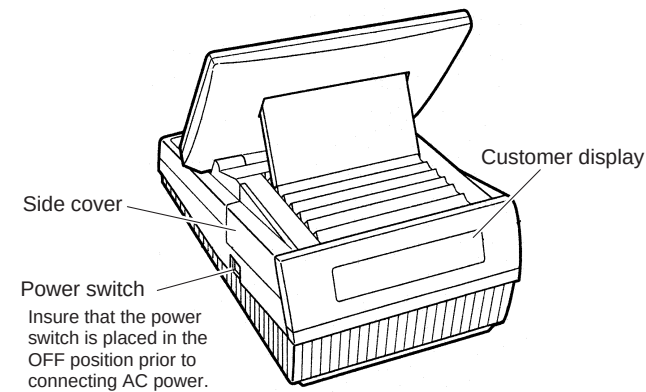
1. Appearance

External view

Front view



Rear view



2. Rating

External dimensions	11.6(W) × 16.3(D) × 12.6(H) in. (295(W) × 414.5(D) × 320(H) mm)
Weight	14.6 lbs. (6.6 kg)
Power source	120V AC ± 10% 60 Hz
Power consumption	Stand-by: 27W Operating: 51W (max.)
Working temperatures	32 to 104°F (0 to 40°C)

3. Displays

This POS terminal is equipped with a color LCD operator display and a two-line customer display.

The operator display is a touch panel.

The operations can be performed by touching the screen (that shows keys or items in the receipt window) of the operator display.

1) Operator display (touch panel)

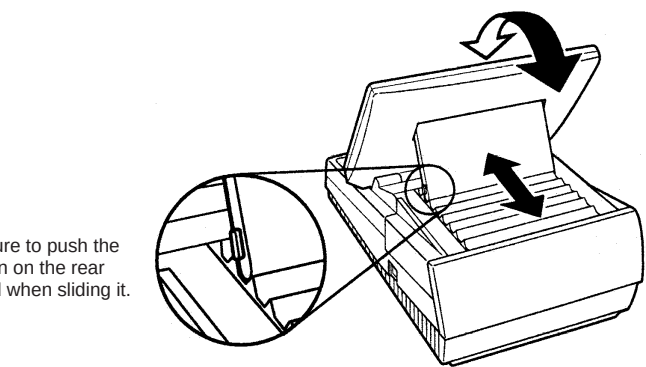
3-1. Display

1) Front display

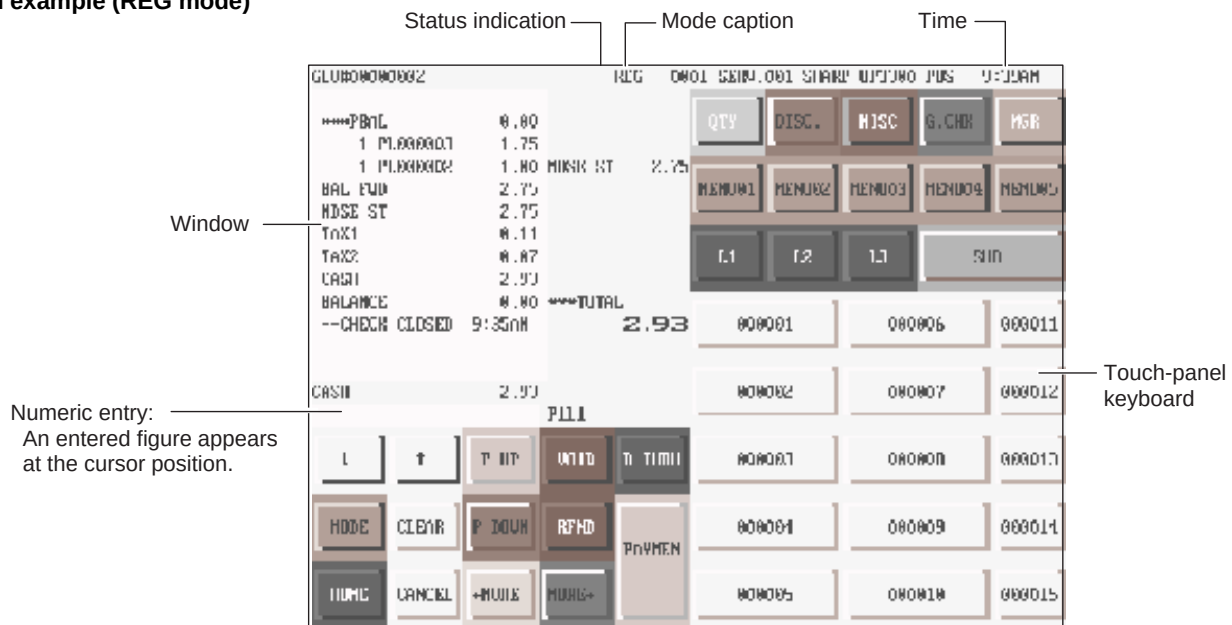
ITEM	SPECIFICATIONS	NOTE
Type	DSTN color LCD with back light	With 256 colors *
Screen size	10.4" Full screen	
Dot format	640 (W) × 480 (H) mm Full dot	
Dot size	0.09 × RGB(W) × 0.31 mm	
Dot space	0.02 mm	

* Note that the application software for the UP-3300 uses 16 colors.

The display can be tilted to the best viewing angle by sliding the rear stand.

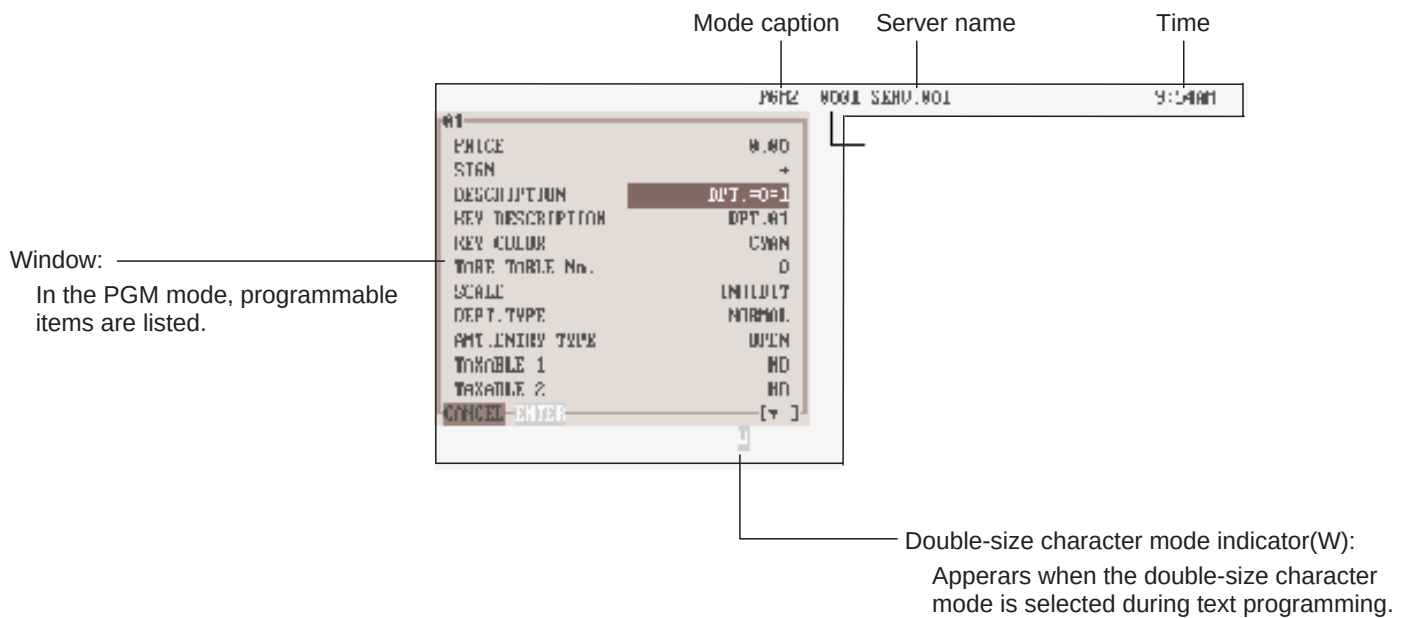


Screen example (REG mode)

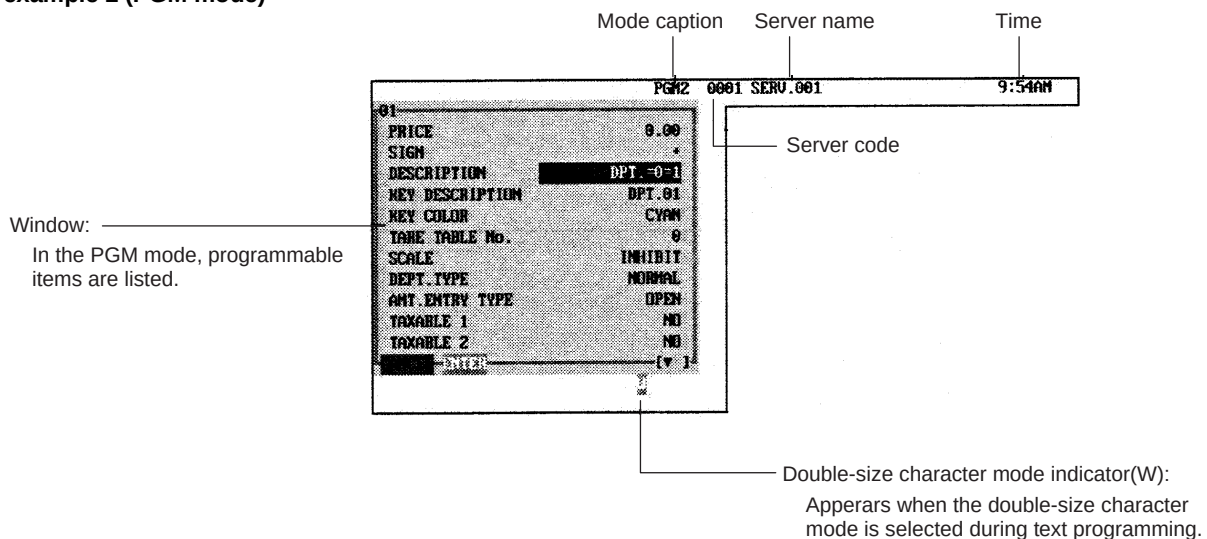


NOTE: The size of a display area depends on the layout of a touch-panel keyboard (ex. key size) or the function mode (ex. drive-through function).

Display example 1 (REG mode)



Display example 2 (PGM mode)



Keyboard layout (default)

- **Home keyboard**

This keyboard appears when touch the **HOME** key.

					QTY	DISC.	MISC	G.CHK	MGR
					MENU01	MENU02	MENU03	MENU04	MENU05
					L1	L2	L3	SUB	
					000001		000006		000011
					000002		000007		000012
↓	↑	P UP	VOID	D-THRU	000003		000008		000013
MODE	CLEAR	P DOWN	RFND	PAYMEN	000004		000009		000014
HOME	CANCEL	←MORE	MORE→		000005		000010		000015

- **Main2 keyboard**

This keyboard appears when you touch the **MORE→** key on the Home keyboard.

					QTY	DISC.	MISC	G.CHK	MGR
					MENU01	MENU02	MENU03	MENU04	MENU05
					L1	L2	L3	SUB	
					000016		000021		000026
					000017		000022		000027
↓	↑	P UP	VOID	D-THRU	000018		000023		000028
MODE	CLEAR	P DOWN	RFND	PAYMEN	000019		000024		000029
HOME	CANCEL	←MORE	MORE→		000020		000025		000030

- **Main3 keyboard**

This keyboard appears when you touch the **MORE→** key on the Function2 keyboard.

					QTY	DISC.	MISC	G.CHK	MGR
					MENU01	MENU02	MENU03	MENU04	MENU05
					L1	L2	L3	SUB	
					000031		000036		000041
					000032		000037		000042
↓	↑	P UP	VOID	D-THRU	000033		000038		000043
MODE	CLEAR	P DOWN	RFND	PAYMEN	000034		000039		000044
HOME	CANCEL	←MORE	MORE→		000035		000040		000045

- **Sub keyboard**

This keyboard appears when you touch the **SUB** key on the Home keyboard.

Home keyboard.

				P1	P2	P3	P4	P5
				COMB01		COMB06		000101
				COMB02		COMB07		000102
				COMB03		COMB08		000103
				COMB04		COMB09		000104
↓	↑	P UP	VOID	COMB05		COMB10		000105
MODE	CLEAR	P DOWN	RFND	PAYMEN			WAIT	
HOME	CANCEL	MORE→						FINAL

- **Sub2 keyboard**

This keyboard appears when you touch the **MORE→** key on the Sub keyboard.

Sub keyboard.

					P1	P2	P3	P4	P5
					COMB11		COMB16		000106
					COMB12		COMB17		000107
					COMB13		COMB18		000108
					COMB14		COMB19		000109
↓	↑	P UP	VOID	SUB	COMB15		COMB20		000110
MODE	CLEAR	P DOWN	RFND	PAYMEN				WAIT	
HOME	CANCEL	← MORE						FINAL	

- **Sub3 keyboard**

This keyboard appears when you touch the **MORE→** key on the Sub2 keyboard.

↓	↑	P UP	VOID	SUB					
MODE	CLEAR	P DOWN	RFND	PAYMEN					
HOME	CANCEL	←MORE	MORE→						

- **Condiment/Menu keyboard**

This keyboard appears when you touch the MENU key in a condiment PLU entry.

The Condiment/Menu2 keyboard appears when you touch the **MORE→** key on the Condiment/Menu keyboard.

The Condiment/Menu3 keyboard appears when you touch the **MORE→** key on the Condiment/Menu2 keyboard.

					KEY001		KEY006		KEY011	
					KEY002		KEY007		KEY012	
					KEY003		KEY008		KEY013	
					KEY004		KEY009		KEY014	
					KEY005		KEY010		KEY015	
↓	↑	P UP	VOID	SUB						
MODE	CLEAR	P DOWN	RFND	PAYMEN			WAIT			
HOME	CANCEL	C NEXT			MORE→		FINAL			

- **Function menu 1 (QTY) keyboard**

This keyboard appears when you touch the **QTY** key on the Home, Main2, or Main3 keyboard.

					X/TIMES				
					7	8	9		
					4	5	6		
↓	↑	P UP			1	2	3		
MODE	CLEAR	P DOWN			0	00	-		
HOME	CANCEL				X/TIMES				

- **Function menu 2 (DISC.) keyboard**

This keyboard appears when you touch the **DISC.** key on the Home, Main2, or Main3 keyboard.

					%1		%5	(-)3	
					%2		%6	(-)4	
					%3		(-)1	(-)5	
					%4		(-)2	(-)6	
					7	8	9	MDS ST	
↓	↑	P UP	VOID	SUB	4	5	6		
MODE	CLEAR	P DOWN	RFND	PAYMEN	1	2	3	MDS ST	
HOME	CANCEL	M.FUNC			0	00	-	PAYMENT MENU	

- **Function menu 3 (MISC) keyboard**

This keyboard appears when you touch the **MISC** key on the Home, Main2, or Main3 keyboard.

					TAX1SF	RLU/SB	WASTE		
					TAX2SF	RCP.SW	REPEAT		
					TAX	RCPT	RP.SND		
					SRV#		MGR#		
					7	8	9		
↓	↑	P UP	VOID	SUB	4	5	6		
MODE	CLEAR	P DOWN	RFND	PAYMEN	1	2	3		
HOME	CANCEL	D-THRU			0	00	-	ENTER	

- **Function menu 4 (G.CHK) keyboard**

This keyboard appears when you touch the **G.CHK** key on the Home, Main2, or Main3 keyboard.

					QTY	DISC.	MISC		MGR
					SRV#		MGR#		
					7	8	9	N.C.	
↓	↑	P UP	VOID	SUB	4	5	6	CVCNT	
MODE	CLEAR	P DOWN	RFND	PAYMEN	1	2	3	PBAL	
HOME	CANCEL	MFUNC			0	00	-	ENTER	

- **Function menu 5 (MGR) keyboard**

This keyboard appears when you touch the **MGR** key on the Home, Main2, or Main3 keyboard.

					EMPL#	SRV#	M.FUNC		
					E.SALE	TIME-IN	WASTE		
					BAL	TIME-OUT	#		
					MGR#	BREAK	NS		
					7	8	9	SBTL	
↓	↑	P UP	VOID	RCP.SW	4	5	6	PAYMENT MENU	
MODE	CLEAR	P DOWN	RFND	RCPT	1	2	3	ENTER	
HOME	CANCEL	RETURN	ST VD	BILL	0	00	-	CASH	

- **Function menu 6 or Function menu 7 keyboard**

This keyboard appears when you touch the **FUNC.6** or **FUNC.7** key on the Home, Main2, or Main3 keyboard.

↓	↑	P UP							
MODE	CLEAR	P DOWN							
HOME	CANCEL								

- **Payment menu (PAYMENT MENU) keyboard**

This keyboard appears when you touch the **PAYMENT MENU** key on the Home, Main2, or Main3 keyboard.

					QTY	DISC.	MISC	WAIT
					CH1		EAT IN1	FINAL
					CH2		EAT IN2	\$5
					CH3		EAT IN3	\$10
					7	8	9	\$20
↓	↑	P UP	VOID	SUB	4	5	6	NEXT\$
MODE	CLEAR	P DOWN	RFND	M.FUNC	1	2	3	SBTL
HOME	CANCEL	STVOID			0	00	-	CASH

- **Drive thru (D-THRU) keyboard**

This keyboard appears when you touch the **D-THRU** key on the Home, Main2, or Main3 keyboard.

↓	↑			N.C.2	WAIT
MODE	CLEAR			PBAL2	RECALL
HOME	CANCEL			SUB	ENTER

- **SRV/PGM/XZ mode keyboard**

This keyboard appears when you touch the **MODE** key on the Home, Main2, or Main3 keyboard.

					↑	P UP	MODE	AUTO21	
					↓	P DOWN	LIST	AUTO22	
					EMPL#		CANCEL	AUTO23	
					SRV#	X/TIME	CLEAR	AUTO24	
					7	8	9	AUTO25	
					4	5	6	NEXT	HOME
					1	2	3	ENTER	
					0	00	-	CASH	

These keys will not appear in the OPXZ,X1,Z1,X2, or Z2 mode.

- **Character keyboard**

This keyboard is used when you need to enter text data during PGM2 mode entries.

INS	DEL	P.DW	↑	P.UP
PREV	NEXT	←	↓	→
CANCEL	B.S	DC		CODE
CLEAR				
ENTER				
			↔	↑/↓
_/+	-/=	:;	[{	]}
1/!	2/@	3/#	4/\$	5/%
6/^	7/&	8/*	9/(	0/)
q/Q	w/W	e/E	r/R	t/T
y/Y	u/U	i/I	o/O	p/P
a/A	s/S	d/D	f/F	g/G
h/H	j/J	k/K	l/L	
z/Z	x/X	c/C	v/V	b/B
n/N	m/M	,/<	>/;	//?
SHIFT			SPACE	
			SHIFT	

Function keys list (default keyboard and labels)

Caption (default)	Function
HOME	Used to return to HOME keyboard.
CANCEL	Used to cancel your current operation or menu or return to previous menu.
CLEAR	Used to clear the entered data (amounts/rates/parameters, etc.) and the error state.
MODE	Used to go to MODE selection window or to return to HOME keyboard.
↑	Used to control the cursor (up arrow).
↓	Used to control the cursor (down arrow).
←MORE	Used to change the keyboard.
→MORE	Used to change the keyboard.
ENTER	Used to select item/menu or entered data.
SUB	Used to go to the sub-keyboard.
CASH	Used to enter the direct cash/amount tendered operation, or to finalize the PGM job.
0 thru 9	Used to enter a numeric data (0 thru 9).
00	Used to enter a numeric data (00).
000	Used to enter a numeric data (000).
•	Used to enter a fractional part, or to toggle between two or more options.
X/TIMES	Used to enter a quantity or time.
SBTL	Used to display subtotals.
P UP	Used to scroll page up.
P DOWN	Used to scroll page down.
BKSPC	Used to backs up the cursor for deleting the character or figure at the left of the cursor.
DEL	Used to delete a character or figure in the cursor position.
MDS ST	Used to display the merchandise subtotal.
TRY ST	Used to display the tray subtotal.
#	Used to enter a non-add code.
NS	Used to execute a no-sale function.
SCALE	Used to enter a weight for the item entry.
PLU/SB	Used to enter a PLU/subdepartment from the list by using a code.
L1 thru L10	Used to shift the direct PLU key level (level 1 thru 10).
P1 thru P5	Used to shift the PLU price level (level 1 thru 5).
TAX1SF	Used to shift the taxability 1.
TAX2SF	Used to shift the taxability 2.
TAX3SF	Used to shift the taxability 3.
TAX4SF	Used to shift the taxability 4.
BILL	Used to print the bill.
RCPT	Used to print the receipt after transaction.
CH TIP	Used to enter the charge tip.
CA TIP	Used to enter the cash tip.
TIP PD	Used to execute the tip paid function.
VOID	Used to void a last item, or used for the cursor void function.
I.VOID	Used to void a past item, or used for the cursor void function.
ST VD	Used to void an entire transaction (subtotal void).
RFND	Used to enter the refund item.
RETURN	Used to enter the returned item.

Caption (default)	Function
%1 thru %9	Used to enter the percent calculation (percent 1 thru 9).
(-)1 thru (-)9	Used to execute the discount entry (discount 1 thru 9).
TAX	Used to enter the manual tax.
CV CNT	Used to enter the cover count.
AUTO to AUTO7	Used to enter the automatic sequencing (auto 1 thru auto 7).
\$5	Used to enter the speed tender (\$5).
\$10	Used to enter the speed tender (\$10).
\$20	Used to enter the speed tender (\$20).
AUTO11 to AUTO25	Used to enter the automatic sequencing (auto 11 thru auto 25).
CA2	Used to enter the cash 2 payment.
CHK thru CHK4	Used to enter the check payment (check 1 thru 4).
CH1 thru CH8	Used to enter the charge payment (charge 1 thru 8).
EMP CH	Used to enter the employee charge payment.
CONV1 to CONV4	Used to creates a subtotal in foreign currency (conversion 1 thru 4).
PBAL	Used to lookup the guest check.
PBAL2	Used to lookup the guest check (for drive-thru function).
N.C.	Used to open a new guest check.
N.C.2	Used to open a new guest check (for drive-thru function).
SRVC	Used to finalize the guest check temporarily.
FINAL	Used to finalize the guest check temporarily (with the tax calculation).
DEPO	Used to enter the deposit.
DEP.RF	Used to return the deposit.
B.T.	Used to enter the bill transfer/bill totalizing.
RA and RA2	Used to enter the received-on-account (RA 1 and 2).
PO and PO2	Used to enter the paid-out (PO 1 and 2).
SRV#	Used to enter the server code.
MGR#	Used to enter the manager code.
EMPL#	Used to enter the employee code.
EATIN1 thru EATIN3	Used to display the eat-in subtotal (eat-in 1 thru 3).
RP SND	Used to send a partial order to the remote printer.
GRT EX	Used to exempt a customer from the gratuity.
OPN TR	Used to enter the open tare.
BAL	Balance key
REPEAT	Used to repeat a last item entry.
TR.OUT	Used to enter the transfer-out function.
TR.IN	Used to enter the transfer-in function.
PERSN#	Used to enter the person number.
I.PAY	Individual payment key
E.SALE	Used to enter the sales for employees.
M.FUNC	Used to display the miscellaneous function menu.
RCP.SW	Used to switch the receipt printing state (ON/OFF).

Caption (default)	Function
WAIT	Used to shift the corresponding guest check to the wait mode (for drive-thru).
RECALL	Used to re-call the corresponding guest check to the registration mode (for drive-thru).
B.S.	Used to separate the bill.
WASTE	Used to enter/release the WASTE mode.
C NEXT	Used to skip the next table of condiments.
TIME-IN	Used to enter time-in operation.
TIME-OUT	Used to enter time-out operation.
BREAK	Break key.
QTY	Used to go to the function menu 1 keyboard (q'ty entry).
DISC.	Used to go to the function menu 2 keyboard (discount/percentage entry).
MISC	Used to go to the function menu 3 keyboard (the miscellaneous function keyboard).
G.CHK	Used to go to the function menu 4 keyboard (guest check entry).
MGR	Used to go to the function menu 5 keyboard (Manager/Server/Employee entry).
FUNC.6	Used to go to the function menu 6 keyboard (empty).
FUNC.7	Used to go to the function menu 7 keyboard (empty).
PAYMENT MENU	Used to go to the payment menu keyboard.
D-THRU	Used to go to the drive-thru menu keyboard (guest check entry for drive-thru).
NEXT\$	Used to enter the next high-dollars (for including-tax subtotal).
MENU01 to MENU50	Used to go to the direct PLU menu (menu 1 thru 50).

2) Customer display

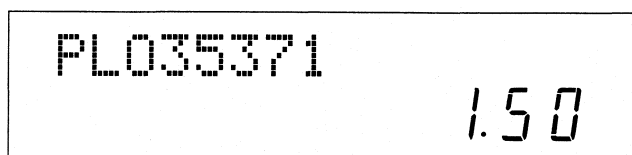
The customer display consists of a 16-position dot-matrix display (upper) and a 11-position 7-segment display (lower).

Lower line

ITEM	SPECIFICATIONS	NOTE
Type	7 Segment type	
Number of digits	11 digits	
Color display	Green	
Character size	12.0(H) × 6.0(W)mm	

Upper line

ITEM	SPECIFICATIONS	NOTE
Type	Dot matrix type	
Number of digits	16 digits	
Color display	Green	
Character size	9.0(H) × 5.6(W)mm	



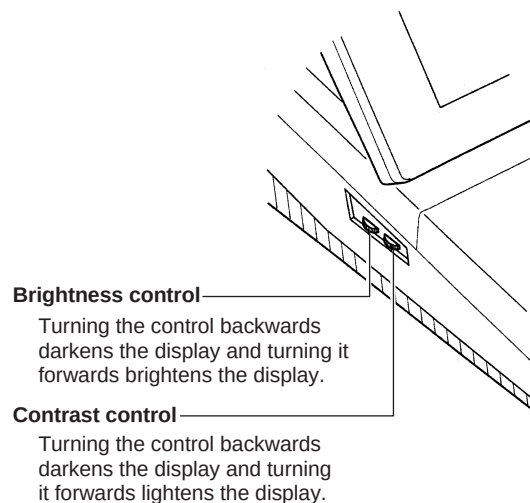
3) Screen save mode

To save electrical power or the display's life, your POS terminal is provided with the screen save function. This function can turn the LCD backlight off when the POS terminal is left idle for an extended period of time. You can program the time for which your POS terminal should keep the normal status (in which the backlight is "ON") before it goes into the screen save mode.

To exit the screen save mode, touch a key.

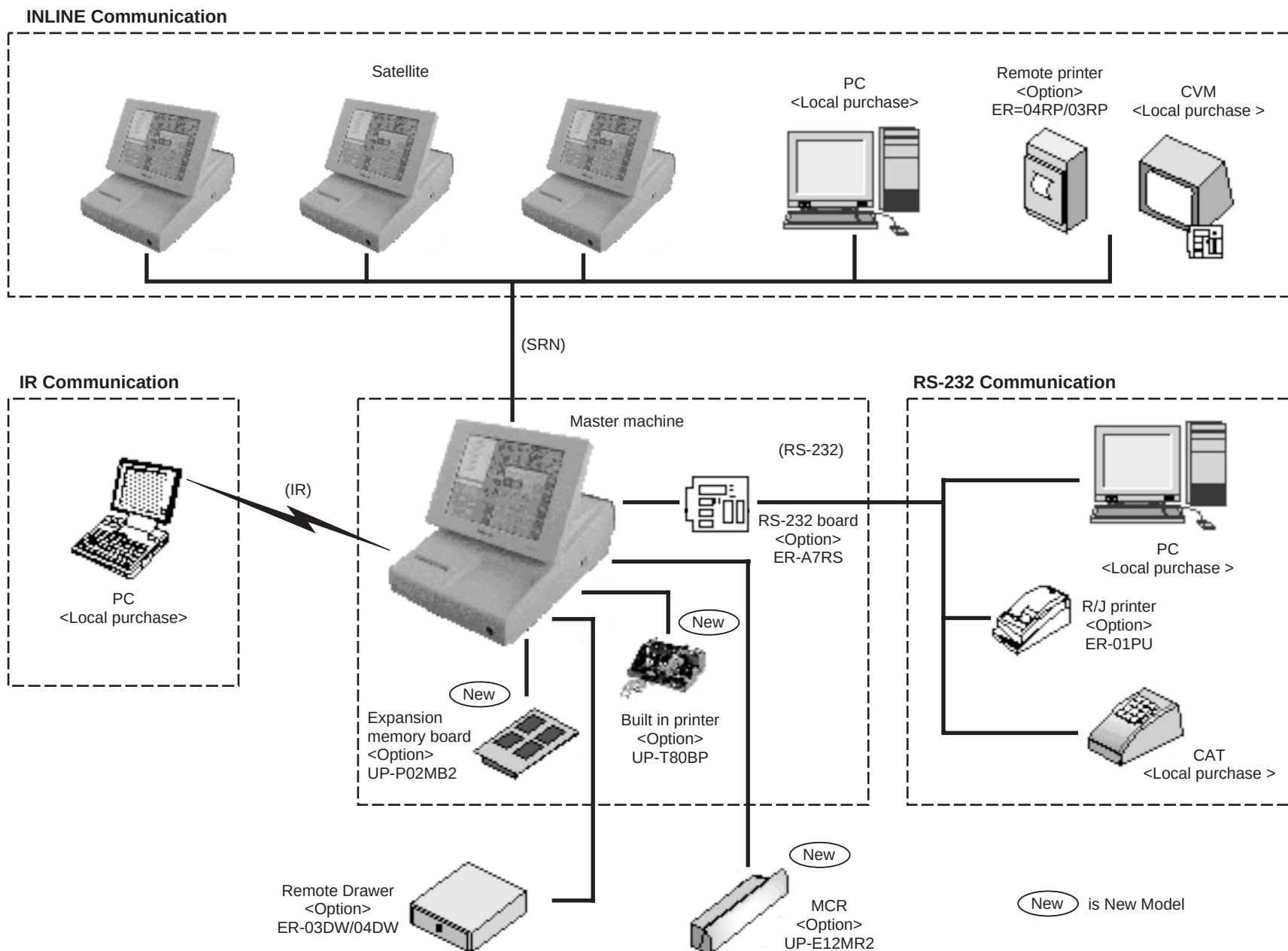
4) Display Adjustment

You can adjustment the brightness and contrast of the display by using the corresponding controls.



CHAPTER 2. OPTIONS

1. System configuration



2. Sales Options

No.	CLASSIFICATION	COMPONENT NAME	MODEL NAME	REMARK
1	Printer	External R/J printer	ER-01PU	Via RS-232 I/F
		Remote printer	ER-03RP	Via SRN I/F
			ER-04RP	
		Built-in printer	UP-T80BP	
2	Drawer	Remote drawer	ER-03DW	
			ER-04DW	
		Coin case	ER-75CC3	7B/5C
			ER-55CC2	5B/5C
3	Memory	Expansion RAM disk board	UP-P02MB2	2M bytes PS-RAM board
4	On-line function	RS232 I/F board	ER-A7RS	2 ports RS232 I/F and MCR I/F
5	Data back up system	Preset loader	ER-02FD	FD unit
		IR I/F	CE-IR2	Wireless I/F for IR communication
			CE-IR4	
6	OTHER	MCR (Magnetic Card Reader)	UP-E12MR2	for ISO 1 & 2 stripe card (Unnecessary ER-A7RS)

3. Local purchase options

No.	COMPONENT NAME	MODEL NAME	
1	CAT terminal	Omni-Series	This equipment will be purchased locally and it will be connected to UP-3300 via RS232 I/F. If standard RS232 2 ports are not available ,ER-A7RS is needed.
		PNC-330	
2	Scale	Toledo, NCI	
3	Coin Dispenser	Telequip Coporation	This equipment will be purchased locally and it will be connected to UP-3300 via SRN and RS232 I/F.
4	Color Kitchen Monitor	Progressive sys.	
5	PC		

4. Service options : None

5. Service tools

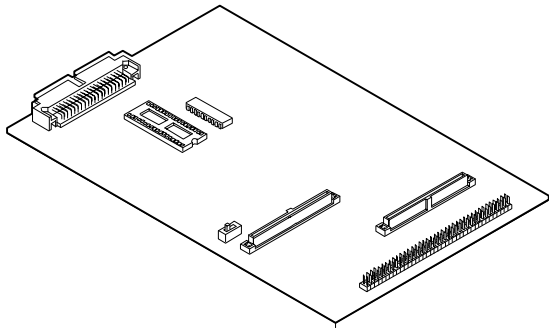
No.	NAME	PARTS CODE	PRICE	DESCRIPTION
1	Terminator(50 Ω)	QCNCM 7 1 4 5 RCZZ	AZ	for SRN in-line system
2	MCR test card	UKOG- 6 7 1 8 RCZZ	BE	for UP-E12MR2
3	RS232 loop back connector	UKOG- 6 7 0 5 RCZZ	BC	for RS232 connector
4	Expansion PWB	CKOG- 6 7 2 4 BHZZ	BX	
5	Printer loop back connector	UKOG- 2 3 5 6 BHZZ	Ⓟ	for UP-T80BP interface

6. Supplies : None

7. How to use service tools

5-1. Expansion PWB : CKOG-6724BHZZ

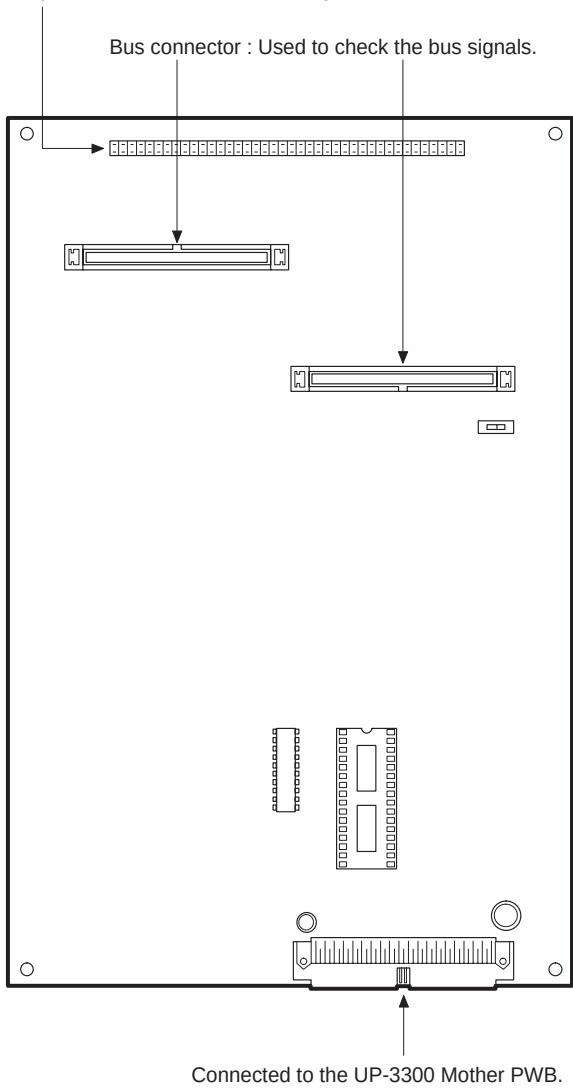
- Extrenal view



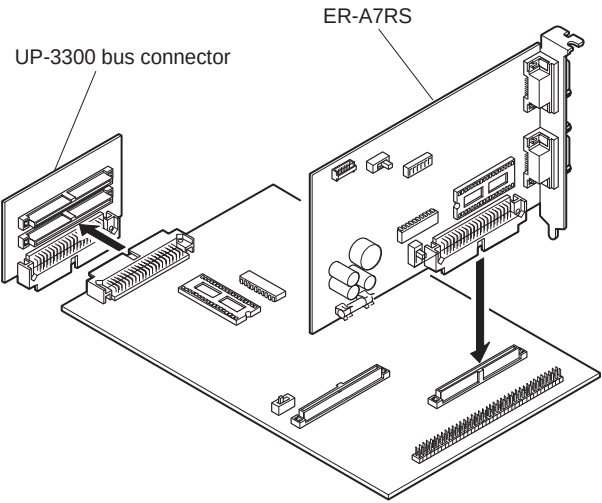
- Plain view

Test pins : Used to check the bus signals.

Bus connector : Used to check the bus signals.



- Connection diagram



5-2. MCR test card: UKOG-6718RCZZ

- Used when executing the diagnostics of the UP-E12MR2.
- External view



CHAPTER 3. SERVICE PRECAUTION

1. Adjustment for SRN (IN-LINE) interface circuit

If transistor Q6 in the transmitter/receiver section has been replaced or if the SRN level requires readjustment, the following alignment is required:

1) Tools and Instruments Required

- ① Oscilloscope (50MHz or better) 1
- ② UP-3300 1

2) Dummy Network Specifications

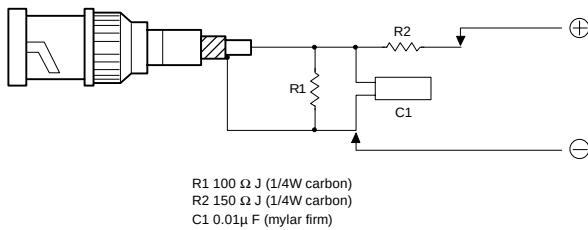


Fig. 1 Dummy network

The oscillator should be connected to the points indicated by $\oplus$ and $\ominus$.

$\oplus$: Connect the positive side of the oscillator.

$\ominus$: Connect the negative side of the oscillator.

3) Connections

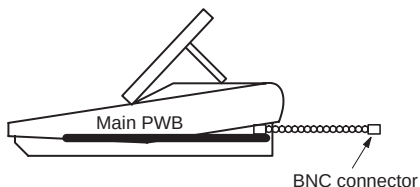


Fig. 2

Attach the BNC connector to the SRN connector (CN2) on the main PWB.

4) Alignment Procedure

① When Using an Oscillator

a) Checking the 1MHz oscillator output

Using an oscilloscope check the 1MHz oscillator's output waveform.

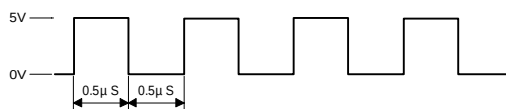


Fig. 3 1MHz oscillator output waveform

NOTE: The oscillator used should have an output impedance of 50 Ω .

b) Connecting the oscillator and its adjustment

Connect a dummy network or branch-trunk network to the output of the SRN connector (CN2), and connect the oscillator to the dummy or branch-trunk network.

* Waveform adjustment

Adjust VR1 until the signal waveform as shown in Fig. 5 is obtained across IC5 (pin 1.5 of the 75115) and GND pin. Turning VR1 clockwise extends the interval of T1.

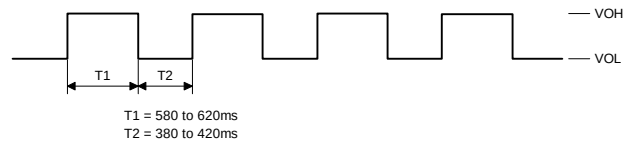


Fig. 5 Receiver regeneration waveform (with dummy network)

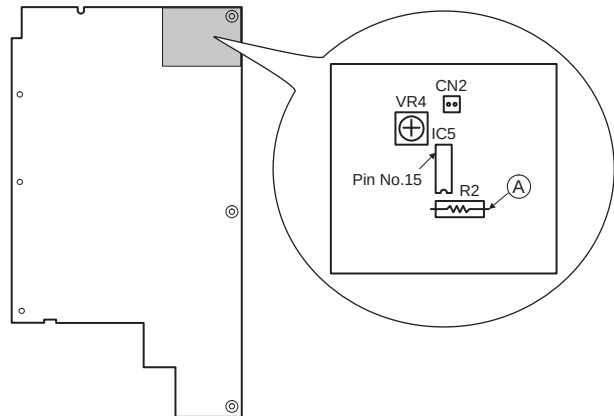


Fig. 6 Board location

2. Calibration

1. Calibration

The coordinates on the touch panel and those on the VGA display may not match for the following reasons.

- The physical deviation between the touch panel and display
- Variations in "electric resistance>coordinate" conversion on the touch panel

Correction of such a deviation is called calibration.

2. Timing of starting calibration

Calibration is started at the following two cases:

– SRV reset/MRS –

1) When touch panel is pressed:

Calibration is started when PROGRAM reset/MRS is performed with the touch panel pressed.

2) When no calibration has been performed:

Calibration is started when the calibration data held by the touch panel controller is broken.

But case 2 isn't performed if case 1 is performed prior to the second.

Calibration is also started when the EEPROM on the touch panel PWB is replaced.

NOTE: If the touch panel unit is replaced for any reason such as a repair, start calibration, following case 1).

3. Calibration specifications

- 1) The character string "Calibration Mode" is displayed.
- 2) If the touch is kept pressed, the machine waits for the finger leaving the touch panel.
- 3) The character string "Touch these crosses" is displayed.

4) Entering correction mode

The command "Entering correction mode" is issued to the touch panel controller.

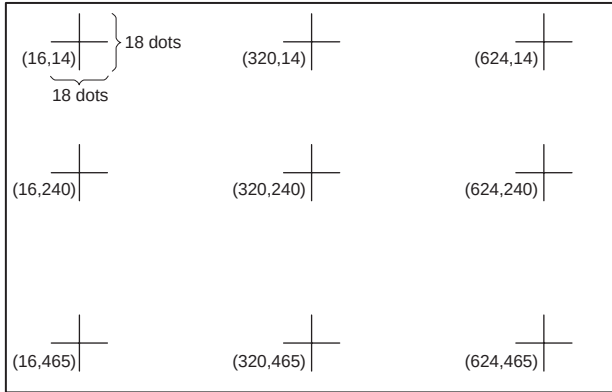
At this step, the coordinate data of the four corners in the input area are passed to the controller.

5) Correction points are displayed

The correction points are displayed.

All of the nine correcting points are displayed as follows using the mark "+". The "+" mark is 18 by 18 dots with 2 dots thick.

VGA Display



6) Correction points are input

Arbitrary correction points are input. Coordinate data corresponding to its input are output from the touch controller. Note the data are those of the initial coordinates. (Refer to the table below.)

The point from where the finger leaves the touch panel is defined as the correction point input position (OFF position).

The data on the nearest correction point is checked, and if almost appropriate, (regarding data of the initial coordinates, within +/-100 dots and +/-5mm in size) the command "correction data set" is issued to the controller. When the panel is released and it is possible to correct with the panel touched, the mark "+" turns green.

If the input coordinates are very far from the correction point, it will be neglected. If the command "correction data set" is terminated normally, the mark "+" at the correction point turns black.

The input coordinate data are those of the initial coordinates, and the relation to the correction points is as follows:

The data of the initial coordinates of correction points

393, 402	2080, 402	3767, 402
393, 2048	2080, 2048	3767, 2048
393, 3697	2080, 3697	3767, 3697

7) Step 6) is repeated for the nine correction points.

Correction is performed in an arbitrary order. At first all of the nine points are displayed in white and they turn black as corrected.

8) After all of the points are corrected, the command "correction mode end" is issued to the controller.

The maximum coordinates are (4096, 4096).

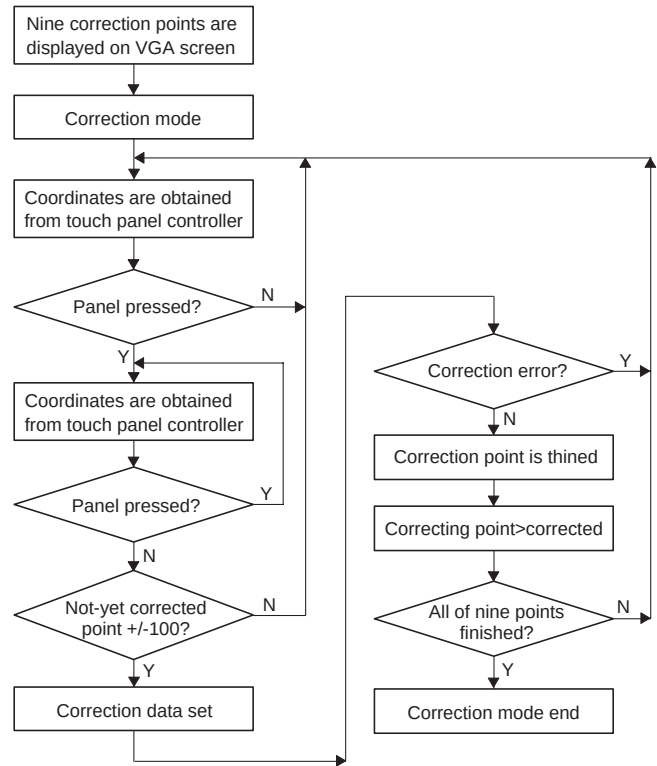
9) The display mode is returned to the text mode.

* If the power supply is turned off during correction, the following messages are displayed and all the steps are started over again.

Calibration failed.

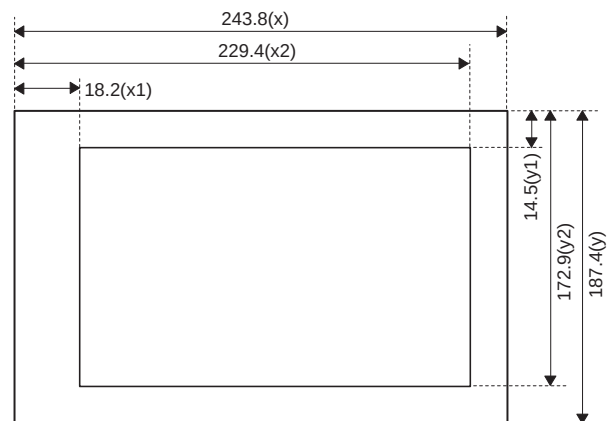
Touch the panel to try again

Calibration flow



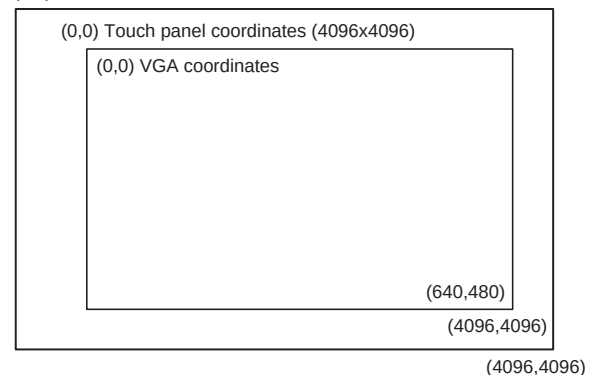
4. Touch panel/VGA coordinates

• Touch panel configuration (unit: mm)



• Touch panel coordinates

(0,0) Initial coordinates



Initial coordinates (xi, yi) ↔ Touch panel coordinates (xt, yt) conversion

$$xt = (xi - 4096 * x1 / x) * (x / (x2 - x1))$$

$$yt = (yi - 4096 * y1 / y) * (y / (y2 - y1))$$

Touch panel coordinates (xt, yt) ↔ VGA coordinates (xv, yv) conversion

$$xv = xt * 640 / 4096$$

$$yv = yt * 480 / 4096$$

- Coordinates of correction points

Initial coordinates

393, 402	2080, 402	3767, 402
393, 2048	2080, 2048	3767, 2048
393, 3697	2080, 3697	3767, 3697

Touch panel coordinates

100, 100	2048, 100	3996, 100
100, 2048	2048, 2048	3996, 2048
100, 3996	2048, 3996	3996, 3996

VGA coordinates

16, 14	320, 14	624, 14
16, 240	320, 240	624, 240
16, 465	320, 465	624, 465

3. IPL (Initial program Loading) function

1) Introduction

The application software of the UP-3300 written in the flash ROM.

In the following cases, writing procedure of the application software into the flash ROM is required

- When the flash ROM is replaced with new one. The service part flash ROM does not include the application software in it.
- When IPL writing is required because of change in the software.
- * The service part of the main PWB unit includes the flash ROM with the application software written in it, and there is no need for writing the application software when replacing the main PWB unit.

2) IPL procedure

There are two ways of IPL procedures.

- IPL from P-ROM via ER-A7RS
- IPL from PC via IR (infrared) communication (Please refer the next section)

The detailed descriptions on the above procedures are given below.

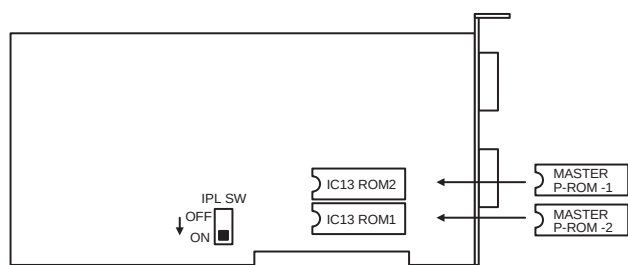
3) IPL from P-ROM via ER-A7RS

- (1) Install the two master ROMs to the IC socket (IC12, IC13) on the ER-A7RS.

Master ROM -1 : VHI27801RADIX

Master ROM -2 : VHI27801RAEIX

- (2) IPL switch on the ER-A7RS : Set the IPL SW to ON position.



- (3) Install the ER-A7RS to the UP-3300. (The UP-3300 power should be turned OFF.)
- (4) Turned on the power of the UP-3300.
- (5) The following display is shown and the IPL procedure is started.

Rear display:

Start:

I	P	L	2	0	-	3	F												
---	---	---	---	---	---	---	---	--	--	--	--	--	--	--	--	--	--	--	--

200000 - 3FFFFFF: Copy address

Check the program version:

I	P	L	2	0	-	3	F												
---	---	---	---	---	---	---	---	--	--	--	--	--	--	--	--	--	--	--	--

Erase the Flash ROM:

I	P	L	2	0	-	3	F												
---	---	---	---	---	---	---	---	--	--	--	--	--	--	--	--	--	--	--	--

Write the program:

I	P	L	2	0	-	3	F												
---	---	---	---	---	---	---	---	--	--	--	--	--	--	--	--	--	--	--	--

No. of Page

Verify the program:

I	P	L	2	0	-	3	F												
---	---	---	---	---	---	---	---	--	--	--	--	--	--	--	--	--	--	--	--

Complete:

OK:

I	P	L	2	0	-	3	F												
---	---	---	---	---	---	---	---	--	--	--	--	--	--	--	--	--	--	--	--

Error:

I	P	L	2	0	-	3	F												
---	---	---	---	---	---	---	---	--	--	--	--	--	--	--	--	--	--	--	--

- (6) Turn OFF the power of the UP-3300.
- (7) Remove the ER-A7RS from the UP-3300.
- (8) Perform the Master reset .

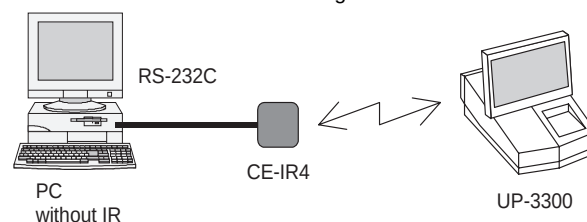
4. UTL33.EXE (UP-3300 Series Utility tool)

1. Outline

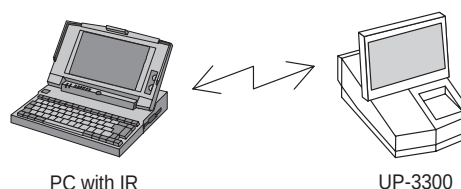
This specification covers the utility program "UTL33.EXE" for UP-3300 series. The "UTL33.EXE" is a program which runs on the PC DOS prompt screen, it is connected to the UP-3300 through IR. It has the following functions: (1) UP-3300 IPL operation; (2) LOGO data rewrite for built-in printer UP- T80BP; and (3) program rewrite.

2. System requirements

PC and UP-3300 are connected through IR.



1. PC + CE-IR4 system



2. PC only system

Fig 1. Connection between PC and UP-3300

3. Functions

The following three functions become available:

- (1) UP-3300 program rewrite (IPL)

The UP-3300 program is updated. S-type files or ER01FD type data files are used for ROM data.

(2) LOGO data rewrite

The LOGO STAMP data for the UP-T80BP is set.

Black-and-white BMP/PCX data is used and the image size is up to 576x240 dots.

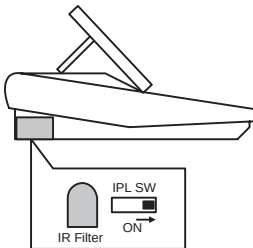
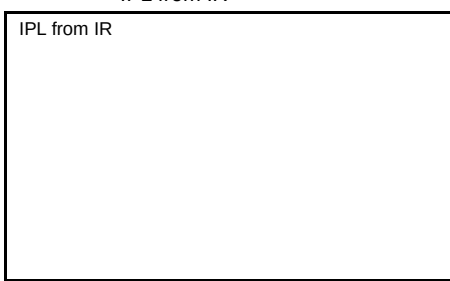
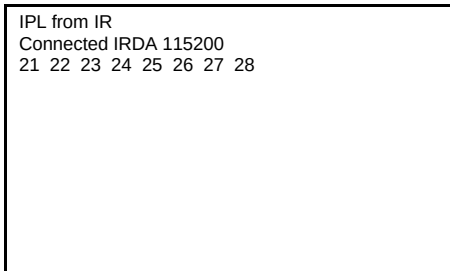
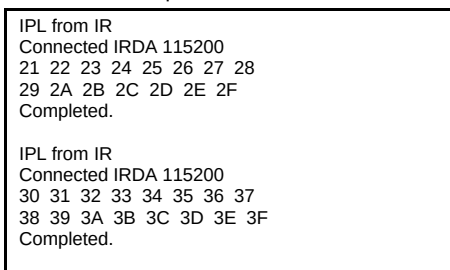
(3) Program rewrite (IPL)

The UP-T80BP program is updated. S-type files are used for ROM data.

According to the contents of the file, "UTL33.EXE" automatically selects the appropriate protocol from the three types described above. 1

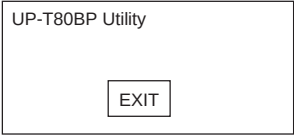
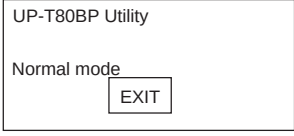
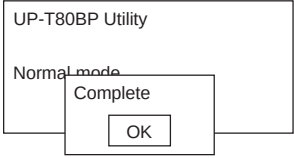
4.

4.1 UP-3300 IPL

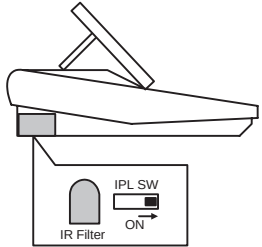
No	Procedure on P.C. side	No	Procedure on UP-3300 side
1	Install "UTL33.EXE" on the P.C.		
		2	Turn OFF the power.
		3	Select "IPL Mode". Set "IPL Switch" of UP-3300 to "ON". 
		4	Turn ON the power.
		5	Starting of "IPL Mode". UP-3300 shows "IPL from IR" 
6	Connect P.C. and UP-3300 via IR. (Fig 1)		
7	Execute "UTL33.EXE" on P.C. Operation: >UTL33 3300_1.ROM 3300_2.ROM ("3300_1.ROM" and "3300_2.ROM" are file name of S-type ROM object.)		
8	Program data is sent to UP-3300 automatically.	8	Program data is received from P.C. automatically. UP-3300 shows 
9	"UTL33.EXE" is completed. P.C. shows "Completed."	9	UP-3300 shows "Completed." 
		10	Turn OFF the power.

No	Procedure on P.C. side	No	Procedure on UP-3300 side
		11	Select "Normal Mode". Set "IPL switch" to "OFF".
		12	Execute "Service Reset" on UP-3300.

4.2 UP-T80BP LOGO

No	Procedure on P.C. side	No	Procedure on UP-3300 side
1	Install "UTL33.EXE" on the P.C.		
		2	Enter the SRV mode. Then turn OFF the power of UP-3300.
		3	While pressing the On-Line key, turn ON the power of UP-3300. Keep pressing the On-Line key, and then press the Feed key also. (Don't move a finger from the On-line key.)
		4	UP-T80BP enters into LOGO mode. UP-T80BP prints out "*****".
		5	Go into "UP-T80BP Utility mode". Select "6 UP-T80BP Utility" in SRV mode.
		6	Starting of "UP-T80BP Utility mode". UP-3300 shows 
7	Connect P.C. and UP-3300 via IR. (Fig 1)		
8	Execute "UTL33.EXE" on P.C. Operation: >UTL33 LOGO.BMP ("LOGO.BMP" is a file name of Bit-Map image.)		
9	Program data is sent to UP-3300 automatically.	9	Program data is received from P.C. automatically. 
10	"UTL33.EXE" is completed. P.C. shows "Completed."	10	UP-3300 shows "Completed."  And UP-T80BP prints out the LOGO image.
		11	Touch "OK" button.
		12	Touch "EXIT" button.
		13	Turn OFF the power of UP-3300.
		14	Execute "Master Reset" on UP-T80BP.

4.3 UP-T80BP IPL

No	Procedure on P.C. side	No	Procedure on UP-3300 side
1	Install "UTL33.EXE" on the P.C.		
		2	Turn OFF the power of UP-3300.
		3	Select "IPL Mode" on UP-T80BP. Set the Bit 1 of DipSwitch 2 to "ON" to enter "IPL Mode". 

No	Procedure on P.C. side	No	Procedure on UP-3300 side
		4	While pressing both the Feed key and the On-Line key, turn ON the power of UP-3300. The ERROR Lamp and the On-line Lamp of UP-T80BP is blinking.
		5	UP-T80BP enters into IPL mode when the Feed key is pressed. (UP- T80BP clears the application program which is in its own flash ROM.) The ERROR Lamp is blinking and the On-Line Lamp is turned off.
		6	UP-T80BP waits the application program data. The ERROR Lamp is turned off and the On-Line Lamp is turned on.
		7	Enter "UP-T80BP Utility" mode. Select "6 UP-T80BP Utility" in SRV mode
		8	Starting of "UP-T80BP Utility" mode. UP-3300 shows UP-T80BP Utility EXIT
9	Connect P.C. and UP-3300 via IR. (Fig 1)		
10	Execute "UTL33.EXE" on P.C. Operation: >UTL33 T80BP.ROM ("T80BP.ROM" is a file name of S-type object.)		
11	Program data is sent to UP-3300 automatically.	11	Program data is received from P.C. automatically. UP-T80BP Utility IPL mode EXIT The On-line Lamp of UP-T80BP starts blinking.
12	"UTL33.EXE" is completed. P.C. shows "Completed."	12	ER-3300 shows "Completed." UP-T80BP Utility IPL mode Complete OK The On-line Lamp of UP-T80BP stops blinking.
		13	Touch "OK" button.
		14	Touch "EXIT" button.
		15	Turn OFF the power of UP-3300.
		16	Select "Normal Mode" on UP-T80BP. Set the Bit 1 of DipSwitch 2 to "OFF" to enter "Normal Mode".
		17	Execute "Master Reset" on UP-T80BP.

<Usage of "UTL33.EXE">

"UTL33.EXE" is a utility program on P.C. - a program that sends the application program data of UP-3300, the image data of the Logo stamp of UP-T80BP or the application program data of UP-T80BP in order to replace them.

Syntax

UTL33 [-Fn] [-Cn] filename [filename ...]

Parameter

filename

Specifies the name file which you want to send.

For UP-3300 IPL S-type ROM object file

For UP-T80BP LOGO STAMP BMP/PCX file

For UP-T80BP IPL S-type ROM object file

Switches

-Fn

Specifies the function. Valid values for n are in the range 1 through 3.

1: UP-3300 IPL

2: UP-T80BP LOGO STAMP

3: UP-T80BP IPL

Normally, UTL33.EXE takes the suitable function automatically. If the automatic selection does not work correctly, please use this switch.

-Cn

Specifies the number of the serial (COM) port. Valid values for n are in the range 1 through 2.

The default value is 1 (COM1).

Example

For UP-3300 IPL.

UTL33 3300_1.ROM 3300_2.ROM

For UP-T80BP LOGO STAMP (To use COM2).

UTL33 -C2 LOGO.BMP

For UP-T80BP IPL (To use the switch "-F").

UTL33 -F3 80BP.ROM.

5. Conditions for soldering circuit parts

To solder the following parts manually, follow the conditions described below.

PARTS NAME	PARTS CODE	LOCATION	CONDITIONS FOR SOLDERING
Ceramic oscillator	RCRMZ 7 0 0 2 RCZZ	MAIN PWB: X1 (8M)	270°/3sec.
	RCRMZ 7 0 0 4 RCZZ	MAIN PWB: X2 (7.37M)	270°/3sec.

6. Note for handling of Touch panel

- The transparency of the touch panel should be vitally important. Do not put finger prints or water print on the surface. Use clean finger such or gloves and masks.
- For handling, do not hold the transparent are, and do not hold the heat seal connector section to assure reliability.
- Do not overlay touch panels. The edge may damage the surface.
- Do not put a heavy thing on the touch panel.
- Do not apply a strong shock, and do not drop it.
- When attaching the protection film again, carefully check for no dirt. If there is any dirt, it is transferred.
- To clean dirt on the surface, use dry, soft cloth or a cloth immersed in ethyl alcohol.
- Check that the housing does not give stress to the touch panel.
- Be careful not to touch the touch panel with tools.
- The heat seal section is easily disconnected. Be careful not to give a stress to the heat seal section when installing.
- The touch panel is provided with an air groove to make the external and the internal air pressure equal to each other. If water or oil is put around the air groove, it may penetrate inside. Be careful to keep the air groove away from water and oil.
- Input is performed with fingers. Do not use a hard thing for inputting.

7. Note for handling of LCD

- The LCD elements are made of glass. BE careful not to give them strong mechanical shock, or they may be broken. Use extreme care not to break them.
- If the LCD element is broken and the liquid is leaked, do not lick it. If the liquid is attached to your skin or cloth, immediately clean with soap.
- Use the unit under the rated conditions to prevent against damage.
- Be careful not to drop water or other liquid on the display surface.
- The reflection plate and the polarizing plate are easily scratched. BE careful not to touch them with a hard thing such as glass, tweezers. Never hit, push, or rub the surface with hard things.
- When installing the unit, be careful not to apply stress to the LCD module. If an excessive stress is applied, abnormal display or uneven color may result.

8. Cautions on handling connectors

When connecting or disconnecting the following connectors, follow the procedures below.

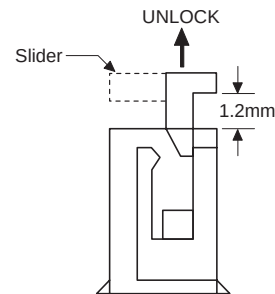
1)

PARTS NAME	PARTS CODE	LOCATION
FFC CONNECTOR	QCNCW 7 2 0 7 RC 4 J	MAIN PWB: CN6 TOUCH PWB: CN5
FFC CONNECTOR	QCNCW 7 1 8 3 BH 2 F	MAIN PWB: CN1

• How to Connect or Disconnect FFC

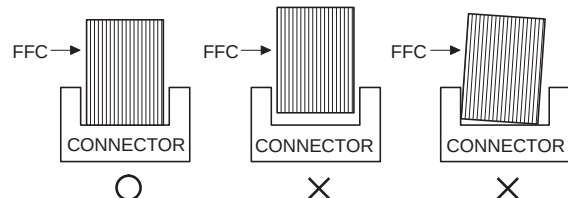
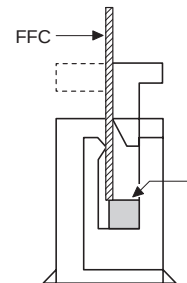
(1) Open the slider to unlock position

The slider will open only up to a fixed height (about 1.2mm). If you forcibly pull up the slider further, it may be dropped.



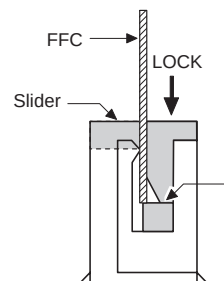
(2) Insert the FFC

Insert the FFC firmly until the FFC hits the bottom of the connector's insulator.



(3) Close the slider to lock position

Insert the FFC and then push the slider downward.

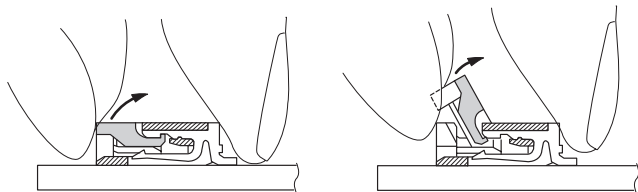


2)

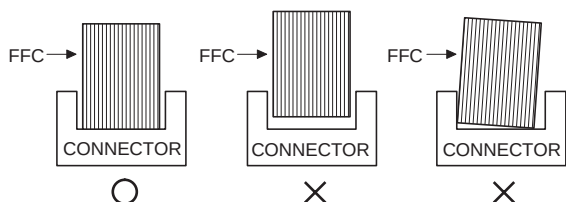
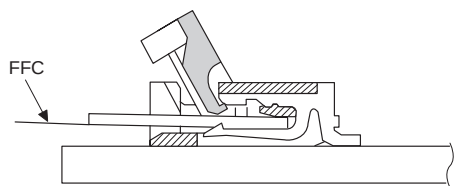
PARTS NAME	PARTS CODE	LOCATION
FFC CONNECTOR	QCNCW7 21 7RC3 J	TOUCH PWB: CN1

• How to Insert FFC

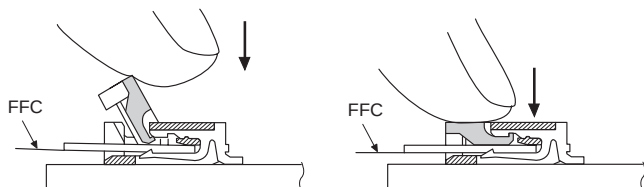
- (1) Open the slider to unlock position
Open the slider upwards up to an angle of 60 degrees. If the slider does not fully open, the FFC can not be smoothly inserted.



- (2) Insert the FFC
Insert the FFC firmly until the FFC hits the bottom of the connector's insulator.



- (3) Close the slider to lock position
Insert the FFC and then push the slider downward.



- (4) To pull out the FFC, unlock the slider to pull it out in the same procedures as (1).

9. Note for handling Rear Display PWB unit

SYSTEM RESET is controlled by the battery-protected CKDC9 (1 chip microcomputer) on the rear display PWB. RESET control becomes impossible if the connection cable leading to the MAIN PWB.

Don't disconnect the CABLE when repairing and adding OPTION.

If it is needed to disconnect the CABLE or it is disconnected by mistake, connect again and carry out SRV RESET.

CHAPTER 4. PROGRAM RESET and SRV mode

In the UP-3300, the following reset switch (location No: S1) is used to switch to the service (SRV) mode and to reset.

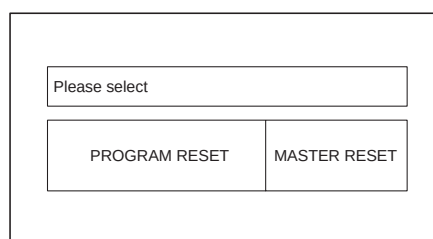
PROGRAM RESET

Used to return the machine back to its operation state after a lock up has occurred.

PROCEDURE

- 1) Turn off the AC switch.
- 2) Set the reset switch to "ON" position.
- 3) Turn on the AC switch.
- 4) Set the reset switch to "OFF" position.
- 5) The reset menu window is displayed as shown below.

DISPLAY:

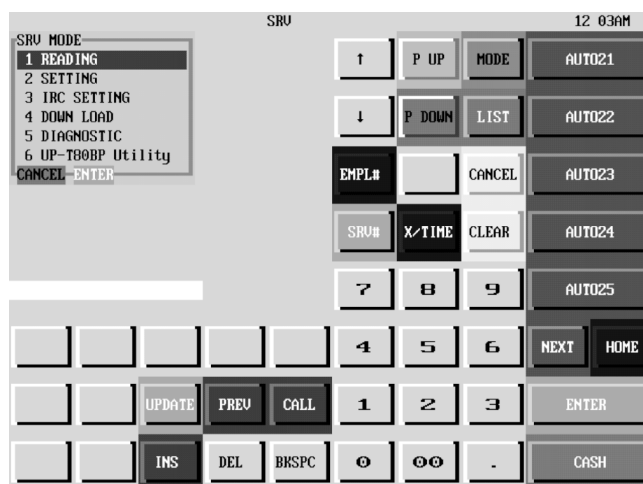


Touch the [PROGRAM RESET] key.

- 6) PROGRAM RESET is started.
- 7) After completion of the program reset, the SRV mode is displayed as shown below.

DISPLAY:

[SRV mode screen]



CHAPTER 5. MASTER RESET (All Memory Clear)

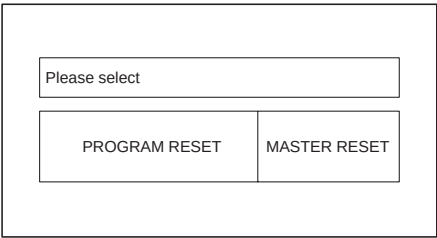
There are three possible methods to perform a master reset.

1. MRS-1 (Master resetting 1): Clear the entire memory and resumes initial values.

PROCEDURE

- 1) Turn off the AC switch.
- 2) Set the reset switch to "ON" position.
- 3) Turn on the AC switch.
- 4) Set the reset switch to "OFF" position.
- 5) The reset menu window is displayed as shown below.

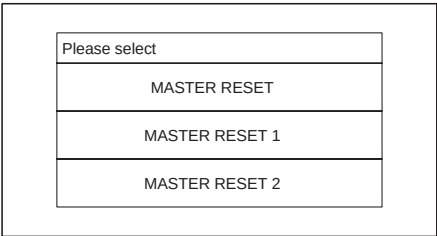
DISPLAY:



Touch the [MASTER RESET] key.

- 6) The master reset menu window is displayed as shown below.

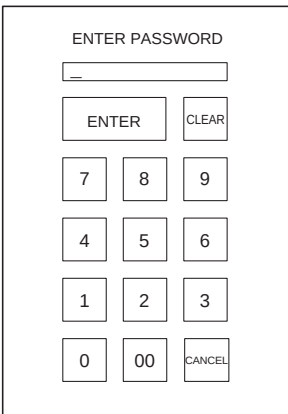
DISPLAY:



Touch the [MASTER RESET] key.

- 7) The secret number input window is displayed as shown below.

DISPLAY:



Enter the secret number for the MASTER RESET-1 and touch the [ENTER] key.

Secret number for MRS-1: 11111111

- 8) MASTER RESET-1 is started.

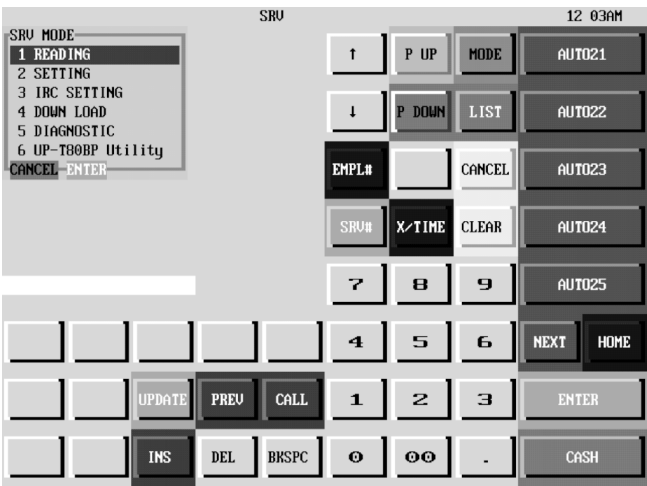
DISPLAY:



- 9) After completion of the master reset, the buzzer sounds three times and the following SRV mode display is shown.

DISPLAY:

[SRV mode screen]



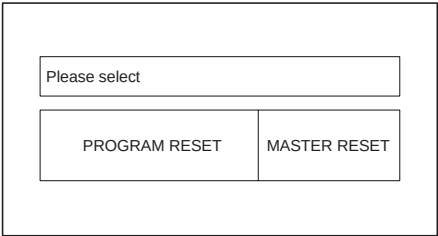
2. MRS-2 (Master resetting 2): Clear the entire memory and resumes initial values.

The keyboard must be entered by hand This reset is used if an application needs different kyeboard layout other than that supplied by a normal MRS-1.

PROCEDURE

- 1) Turn off the AC switch.
- 2) Set the reset switch to "ON" position.
- 3) Turn on the AC switch.
- 4) Set the reset switch to "OFF" position.
- 5) The reset menu window is displayed as shown below.

DISPLAY:



Touch the [MASTER RESET] key.

- 6) The master reset menu window is displayed as shown below.
DISPLAY:

Please select

MASTER RESET

MASTER RESET 1

MASTER RESET 2

Touch the [MASTER RESET 2] key.

- 7) The secret number input window is displayed as shown below.
DISPLAY:

ENTER PASSWORD

ENTER

CLEAR

7	8	9
4	5	6
1	2	3
0	00	CANCEL

Enter the secret number for the MASTER RESET-2 and touch the [ENTER] key.

Secret number for MRS-2: 22222222

- 8) Set the fixed keys in the table below (Start from the [HOME] key, The key are displayed sequentially)
DISPLAY:

ENTER HOME

No.	KEY NAME
1	HOME
2	CANCEL
3	CL
4	MODE
5	UP (↑)
6	DOWN (↓)

- 9) MASTER RESET-2 is started.
DISPLAY:

MASTER RESET

- 10) After completion of the master reset, the buzzer sounds three times and the following SRV mode display is shown.
DISPLAY:

[SRV mode screen]

SRV MODE
SRV
12 03AM

1 READING
2 SETTING
3 IRC SETTING
4 DOWN LOAD
5 DIAGNOSTIC
6 UP-T98BP Utility
CANCEL-ENTER

↑	P UP	MODE	AUTO21
↓	P DOWN	LIST	AUTO22
EMPL#		CANCEL	AUTO23
SRV#	X/TIME	CLEAR	AUTO24
7	8	9	AUTO25
4	5	6	NEXT HOME
UPDATE	PREV	CALL	1 2 3 ENTER
INS	DEL	BKSPC	0 00 - CASH

3. MRS-3 (Master resetting 3): Master resetting 3: Master resetting 3 requires the entry of Serial No. in addition to master resetting 1.

After complete the MRS3, following operations and programming will be inhibited.

1. GT programming.
2. All Memory Download via RS-232C and IR.
3. GT resets with Z report. (Z report can be made, but GT will not be reset.)

PROCEDURE

- 1) Turn off the AC switch.
- 2) Set the reset switch to "ON" position.
- 3) Turn on the AC switch.
- 4) Set the reset switch to "OFF" position.
- 5) The reset menu window is displayed as shown below.
DISPLAY:

Please select

PROGRAM RESET

MASTER RESET

Touch the [MASTER RESET] key.

- 6) The master reset menu window is displayed as shown below.
DISPLAY:

Please select

MASTER RESET

MASTER RESET 1

MASTER RESET 2

- Touch the [MASTER RESET 3] key.
- 7) The secret number input window is displayed as shown below.
DISPLAY:

ENTER PASSWORD

ENTER

CLEAR

7

8

9

4

5

6

1

2

3

0

00

CANCEL

- Enter the secret number for the MASTER RESET-3 and touch the [ENTER] key.
- Secret number for MRS-3: 33333333

- 8) The product serial No. input window is displayed as shown below.
DISPLAY:

SRV

12:41AM

INS

DEL

P.DW

↑

P.UP

PREV

NEXT

←

↓

→

SERIAL No.

CANCEL

ENTER

CANCEL

B.S

DC

CODE

CLEAR

ENTER

→

↑

←

↓

;

[

]

1

2

3

4

5

6

7

8

9

0

q

w

e

r

t

y

u

i

o

p

a

s

d

f

g

h

j

k

l

z

x

c

v

b

n

m

,

.

/

SHIFT

SHIFT

- Enter the product serial No. of this POS and touch the [ENTER] key.

- 9) Set the fixed keys in the table below (Start from the [HOME] key, The key are displayed sequentially)
DISPLAY:

ENTER HOME

No.	KEY NAME
1	HOME
2	CANCEL
3	CL
4	MODE
5	UP (↑)
6	DOWN (↓)

- 10) MASTER RESET-3 is started.
DISPLAY:

MASTER RESET

- 11) After completion of the master reset, the buzzer sounds three times and the following SRV mode display is shown.
DISPLAY:

[SRV mode screen]

SRV MODE

12 03AM

1 READING

2 SETTING

3 IRC SETTING

4 DOWN LOAD

5 DIAGNOSTIC

6 UP-T80BP Utility

CANCEL

ENTER

↑

P UP

MODE

AUTO21

↓

P DOWN

LIST

AUTO22

EMPL#

CANCEL

AUTO23

SRV#

X/TIME

CLEAR

AUTO24

7

8

9

AUTO25

4

5

6

NEXT

HOME

UPDATE

PREV

CALL

1

2

3

ENTER

INS

DEL

BKSPC

0

00

.

CASH

CHAPTER 6. DIAGNOSTICS SPECIFICATIONS

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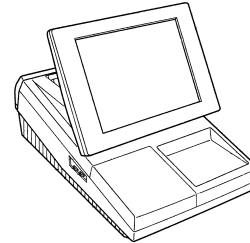
1. General

This diagnostics program is used for simplified checking of the UP-3300 series operations in servicing.
The diagnostics program is built in the standard ROM.

2. System configuration

2-1. Test system

UP-3300 only



3. Diagnostics

Starting the diagnostics

This diagnostics program is written in the external ROM and executed by the CPU (H8/510). To operate this program, the following conditions must be satisfied.

- ① The power for the logic system is proper.
(+5V, VRAM, VCKDC, POFF, +24V)
- ② The input/output pins and the internal logic of the CPU are normal.
In addition, CKDC9, MPCA8, the system bus, and the standard ROM/RAM are normal.

Note: When booting the set for the first time after change the touch panel and EE-PROM, carry out TOUCH KEY CALIBRATION and MASTER RESETING.

In order to add an option unit when the machine is normally operating, perform the program reset in the case of the ER-A7RS and a master reset in case of the UP-P02MB2.

1) Master reset procedure

- ① Turn off the power.
- ② Set the CKDC reset switch to RESET position.
- ③ Turn on the power.
- ④ While touching the touch panel, place the CKDC RESET SWITCH to normal position. (When both the touch panel and EE-ROM was replaced.)
- ⑤ Carry out CALIBRATION. (When both the touch panel and EE-ROM was replaced.)
- ⑥ Select MASTER RESET from the menu and execute.

2) Program reset (service reset) procedure

- ① Turn off the power.
- ② Set the CKDC reset switch to RESET position.
- ③ Turn on the power.
- ④ Set the CKDC reset switch to the normal position. (Do not press the touch panel.)
- ⑤ Select PROGRAM RESET from the menu and execute.

3-1. Execution of diagnostics

To start the diagnostics, select "DIAGNOSTICS" in the menu selection in SRV mode.

The DIAG MAIN MENU is started and the following menu screen is displayed. The selected individual diagnostics program is executed. When the individual diagnostics program is completed, the display returns to the menu screen. To terminate the diagnostics, press the CANCEL key. Then the display returns to the SRV mode menu screen.

***** UP-3300 Diagnostics V1.0A *****

Product & Test Diag	IrDA Diag
RAM Diag	Drawer Diag
ROM & SSP Diag	Rear Display Diag
Clock & Clerk Diag	MCR Diag
Touch Panel Diag	Printer Diag
Serial I/O Diag	
LCD Diag	
SRN Diag	Cancel

WARNING: "Product & Test Diagnostics" is used only in the production process, and must be not used in servicing.

3-2. RAM Diagnostics

This diagnostics is used to test the standard RAM and the expansion RAM.

The following menu is displayed. Press the touch key for the of the operation you want to execute to execute individual Diag programs.

Pressing the CANCEL key returns the screen to the Diag MAIN menu.

RAM Diagnostics

Standard RAM Check	
UP-P02MB2 Check	
	Cancel

1) Standard RAM Check

① Check content

For the pseudo SRAM of the standard RAM 1MB, the following check is performed. The memory contents will not be changed by this check.

The following processes are performed for the memory address (700000H ~ 7FFFFFFH) to be checked.

PASS1: Memory data save

PASS2: Data "0000H" write

PASS3: Data "0000H" read/compare, data "5555H" write

PASS4: Data "5555H" read/compare, data "AAAAH" write

PASS5: Data "AAAAH" read/compare

PASS6: Memory data writed the saved data

In case of a compare error in the check sequences of PASS1 ~ PASS6, an error display is made. If there is no error at all, the check is normally terminated.

In addition, the following address check is performed.

In case of an error, an error display is made and read/write of the address where the error occurred is repeated.

Check point address = 700000H, 700001H
700002H, 700004H
700008H, 700010H
700020H, 700040H
700080H, 700100H
700200H, 700400H
700800H, 701000H
702000H, 704000H
708000H, 710000H
720000H, 740000H
780000H

② Display

Standard RAM Check

Standard memory size: 1024KB PASS!!(or ERROR!!)

Error Address xxxxxxH

Write Data xxxxH

Read Data xxxxH

The error address and the bit are displayed only when the error occurs. (If the error does not occur, the error address will not be displayed.)

③ Terminating procedure

After completion of check, press the Touch panel.

2) UP-P02MB2 Check

① Check content

The UP-P02MB2 presence check is performed in the following procedure. The memory contents will not be changed by this check.

- 55AAH is written into 9FFFFFFH.
- 9FFFFFFH is read and compared with 55AAH. If the both data are correct, the following procedure is performed. If not, "Extended RAM size: 0KB" is displayed and the check is terminated.

For the UP-P02MB2, the following check is performed.

The following processes are performed for the check address (800000H ~ 9FFFFFFH).

PASS1: Memory data save

PASS2: Data "0000H" write

PASS3: Data "0000H" read/compare, data "5555H" write

PASS4: Data "5555H" read/compare, data "AAAAH" write

PASS5: Data "AAAAH" read/compare

PASS6: Memory data writed the saved data

In case of a compare error in the check sequences of PASS1 ~ PASS6, an error display is made. If there is no error at all, the check is normally terminated.

In addition, the following address check is performed in the above check sequence.

In case of an error, an error display is made and read/write of the address where the error occurred is repeated.

Check point address = 800000H, 800001H
800002H, 800004H
800008H, 800010H
800020H, 800040H
800080H, 800100H
800200H, 800400H
800800H, 801000H
802000H, 804000H
808000H, 810000H
820000H, 840000H
880000H, 900000H

② Display

UP-P02MB2 Check

Extended RAM size : 2048KB PASS!!(or ERROR!!)

Error Address xxxxxxH
Write Data xxxxH
Read Data xxxxH

The error address and the bit are displayed only when the error occurs. (If the error does not occur, the error address will not be displayed.)

③ Terminating procedure

After completion of check, press the Touch panel.

3-3. ROM & SSP Diagnostics

The standard ROM and the service ROM are checked. The SSP circuit is also checked.

The following menu is displayed. Press the touch key for of the operation you want to execute to execute individual Diag programs.

Pressing the CANCEL key returns the screen to the Diag MAIN menu.

ROM & SSP Diagnostics

Standard ROM Check	
Service ROM Check	
SSP Check	
	Cancel

1) Standard ROM Check

① Check contents

The standard ROM area (200000H ~ 3FFFFFFH) is added in the unit of byte. If the lower two digits of the result is 20H, it is normal. The ROM version and the model name code which are stored in address 31FFE0H ~ 31FFFFH where the ROM version and the check sum correction data stored are displayed. The format of data (ASCII) to be stored is as follows:

31FFE0H ~ 31FFE0H: Model name code (example: UP-3300, Display is made up to 00H of data.)

31FFF0H ~ 31FFF9H: 27801R****(****=PROGRAM VERSION)

31FFFAH ~ 31FFFBH: BLOCK NO. ("20" ~ "3F")

31FFFC: TERMINATOR ("=")

31FFFDH ~ 31FFFEH: BLOCK VERSION (example "00")

31FFFFH: CHECK SUM CORRECTION DATA

The flash ROM used as the standard ROM has rewriting block of 64KB as the unit. To control the version in each block, the composition is the same as the above 31FFF0H or later and arranged in each 64KByte. At that time, correction is made so that the sum of each block becomes 01H, and the total of 2MByte is 20H.

The FLASH write MASTER EPROM has changed from 8 Mbits to 2 chips so that the program version indication can be managed by each chip. The program version stored in the blocks of 21H and 31H is displayed.

The program version of the IPL is displayed so that 0PAGE where the IPL is stored is individually controlled.

② Display

Standard ROM Sum Check : PASS!!(or ERROR!!)

IPL PROGRAM Version

** ← Display the version.

APL PROGRAM Version

27801R**** UP-3300

27801R**** UP-3300

BLOCK Version

20=** 21=** 22=** 23=** 24=** 25=** 26=** 27=**

28=** 29=** 2A=** 2B=** 2C=** 2D=** 2E=** 2F=**

30=** 31=** 32=** 33=** 34=** 35=** 36=** 37=**

38=** 39=** 3A=** 3B=** 3C=** 3D=** 3E=** 3F=**

③ Terminating procedure

After displaying the check result, press the Touch panel to terminate the check.

2) SERVICE ROM Check

Note: This check should only be performed will be using the service ROM.

① Check content

The standard ROM (EPROM × 2 Chip) area (D00000H ~ EFFFFFFH) is added in the unit of byte. If the lower two digits of the result is 10H, it is normal. The ROM version and the model name code which are stored in address D1FFE0H ~ D1FFFFH where the ROM version and the check sum correction data are stored are displayed. The format of data (ASCII) to be stored is as follows:

D1FFE0H ~ D1FFE0H: Model name code (example: UP-3300, Display is made up to 00H of data.)

D1FFF0H ~ D1FFF9H: 27801R****(****=PROGRAM VERSION)

D1FFFAH ~ D1FFFBH: BLOCK NO. ("20" ~ "2F")

D1FFFC: TERMINATOR ("=")

D1FFFDH ~ D1FFFEH: BLOCK VERSION (example "00")

D1FFFFH: CHECK SUM CORRECTION DATA

This SERVICE ROM allows to write into the FLASH ROM when re-execution is impossible because of an abnormality during re-writing into the FLASH ROM. The composition is the same as the standard ROM.

The program version of the IPL is displayed so that 0PAGE where the IPL is stored is individually controlled.

② Display

Service ROM Sum Check 1 : PASS!!(or ERROR!!)

Service ROM Sum Check 2 : PASS!!(or ERROR!!)

IPL PROGRAM Version

** ← Display the version.

APL PROGRAM Version

27801R**** UP-3300

27801R**** UP-3300

BLOCK Version

20=** 21=** 22=** 23=** 24=** 25=** 26=** 27=**

28=** 29=** 2A=** 2B=** 2C=** 2D=** 2E=** 2F=**

③ Terminating procedure

After displaying the check result, press the Touch panel to terminate the check.

3) SSP Check

① Check content

By starting this check program, the SSP setting for checking is automatically performed and the SSP check is executed and the result is displayed.

The SSP check sets data for checking in the vacant space of the SSP entry register, and deletes the data that is checked after completion of checking. Therefore, the already set data is not changed by this check.

② Display

SSP Check	
SSP (NMI) Check	: PASS!! (ERROR!!)

③ Terminating procedure

After displaying the check result, press the Touch panel to terminate the check.

3-4. Timer Diagnostics

The operation of the clock crystal of CKDC, and the keyboard are tested.

When the CANCEL key is pressed, the display returns to the diagnostics menu.

1) Timer Check

① Check

The operation of the CKDC9 clock crystal is checked.

The indication "YY/MM/DD & MM:HH:SS" is continuously updated. Check the time updated and indicated.

Timer Diagnostics
DATE & TIMER = YY/MM/DD & HH:MM:SS

3-5 Touch Panel Diagnostics

1) Touch Panel Check

① Check

The input test of the touch panel is as follows: a rectangle of dotted lines is displayed at the corner of the LCD screen in the order of upper right, upper left, lower left, and lower right. Check whether a catch sound is heard and the square turns black when each position is touched.

Touch Panel Diagnostics Touch Cursor!! Cancel
--

② End

The test is over when the four corners have been touched. To exit, please press the touch panel.

3-6. RS232 I/F Diagnostics

The main PWB and the option PWB (RS232 interface of ER-A7RS) are checked. Attach the 9-pin D-Sub loop back connector (UKOG-6717RCZZ) of wiring in Fig. 3-11.

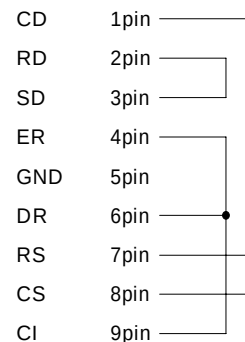


Fig. 3-11. Wiring diagram of loop back connector (UKOG-6717RCZZ)

The following menu is displayed. Press the touch key for the operation you want to execute to execute individual Diag programs.

Pressing the CANCEL key returns the screen to the Diag MAIN menu.

IMPORTANT

When setting channels of RS232, do not set two or more ports to one channel. In the UP-3300, max. two units of ER-A7RS can be installed. In each PWB, do not set two or more ports to the same channel. If two or more ports should be set to the same channel, the hardware can be destroyed.

RS232 I/F Diagnostics	
CHANNEL Check	
CH1 Check	
CH2 Check	
CH3 Check	
CH4 Check	
CH5 Check	
CH6 Check	
	Cancel

1) CHANNEL Check

① Check content

The CHANNEL setting of the connected RS232 is displayed. The display content and the setting of DIP SW for CHANNEL setting on the RS232 I/F PWB are compared.

Since the RS232 and printer port on the main PWB of the UP-3300 is fixed to CH1, CH2 and CH7, that in the ER-A7RS must be set to CH3 ~ CH6.

RS232 I/F Diagnostics	
CHANNEL Check	
CH1 = exist!	← Display when channel present
CH2 = exist!	
CH3 = none!	← Display when no channel
CH4 = none!	
CH5 = none!	
CH6 = none!	
CH7 = exist!	

(Reference) ER-A7RS CHANNEL setting (In the table below, "1" = SW OFF, "0" = SW ON.)

ER-A7RS CON3

S1-1	S1-2	S1-3	CHANNEL
0	0	0	Invalid
0	0	1	CHANNEL 1: Do not set this (Reserved for standard RS)
0	1	0	CHANNEL 2: Do not set this (Reserved for standard RS)
0	1	1	CHANNEL 3
1	0	0	CHANNEL 4
1	0	1	CHANNEL 5
1	1	0	CHANNEL 6
1	1	1	CHANNEL 7: Do not set this (Reserved for internal printer)

ER-A7RS CON4

S1-4	S1-5	S1-6	CHANNEL
0	0	0	Invalid
0	0	1	CHANNEL 1: Do not set this (Reserved for standard RS)
0	1	0	CHANNEL 2: Do not set this (Reserved for standard RS)
0	1	1	CHANNEL 3
1	0	0	CHANNEL 4
1	0	1	CHANNEL 5
1	1	0	CHANNEL 6
1	1	1	CHANNEL 7: Do not set this (Reserved for internal printer)

② Terminating procedure

Press the Touch panel to terminate the check.

2) CH1 Check

① Check content

When the channel is not set, an error display is made (ER-ROR:CH1). When the channel is set, the following check is performed.

- Control signal check

ERn	RSn	DRn	CI n	CDn	CSn
OFF	OFF	OFF	OFF	OFF	OFF
OFF	ON	OFF	OFF	ON	ON
ON	OFF	ON	ON	OFF	OFF
ON	ON	ON	ON	ON	ON

The read check of the above inputs and the interruption check of CS, CI, and CD are performed.

In the read check, ER and RS are changed over in the above sequence and the logic states of DR, CI, CD, and CS are checked.

If the logic differs from that in the table, an error display is made.

"ON" in the table means Active LOW, and "OFF" means Active HIGH.

In the interruption check, an interruption of CS, CI, or CD is allowed one by one. (MASK is canceled.)

If an interruption is not made when each signal is active, or if an interruption is made when each signal is not active, an error display is made.

The above check is repeated four cycles.

- Data transfer check

The loop back data (256 bytes) of 00H ~ 0FFH are used for data transfer check. The baud rate is set to 38400BPS.

- Timer check (RS232 on board timer)

Before performing the check, set the timer to TCVDt start and 5ms. Then perform the following procedure.

* During execution of the check, TRQ- must not be generated.

* After 5ms from completion of the check, TRQ- must be generated.

② Display

RS232 CH1 Check
ER-DR : ERROR!!

All the contents of an error must be displayed.

ERROR No.	ERROR display	ERROR content
1	ER-DR:ERROR	ER-DR LOOP ERROR
2	ER-CI:ERROR	ER-CI LOOP ERROR
3	RS-CD:ERROR	RS-CD LOOP ERROR
4	RS-CS:ERROR	RS-CS LOOP ERROR
5	CI INT:ERROR	CI interruption is not made.
6	CD INT:ERROR	CD interruption is not made.
7	CS INT:ERROR	CS interruption is not made.
8	TXEMP:ERROR	TXEMP is not set.
9	TXEMP INT:ERROR	TXEMP interruption is not made.
10	TXRDY:ERROR	TXRDY interruption is not made.
11	TXRDY INT:ERROR	TXRDY interruption is not made.
12	RCVRDY:ERROR	RCVRDY is not set. (Reception enabled. TR-Q is generated during check)
13	RCVRDY INT:ERROR	RCVRDY interruption is not made.
14	SD-RD:ERROR	SD-RD LOOP ERROR (DATA ERROR)
15	SD-RD:ERROR	SD-RD LOOP ERROR (DATA ERROR, FRAMING ERROR, etc.)
16	TIMER:ERROR	TIMER ERROR (TMRQ is not set after completion of check.)
17	TIMER INT:ERROR	TRQ-1 interruption is not made.

③ Terminating procedure

Press the Touch panel to terminate the check.

3) CH2 Check

① Check content

The check procedure, the display, and the terminating procedure are the same as CH1 Check.

4) CH3 Check

① Check content

The check procedure, the display, and the terminating procedure are the same as CH1 Check.

5) CH4 Check

① Check content

The check procedure, the display, and the terminating procedure are the same as CH1 Check.

6) CH5 Check

① Check content

The check procedure, the display, and the terminating procedure are the same as CH1 Check.

7) CH6 Check

① Check content

The check procedure, the display, and the terminating procedure are the same as CH1 Check.

3-7. Liquid Crystal Display Diagnostics

The UP-3300 LCD display is checked.

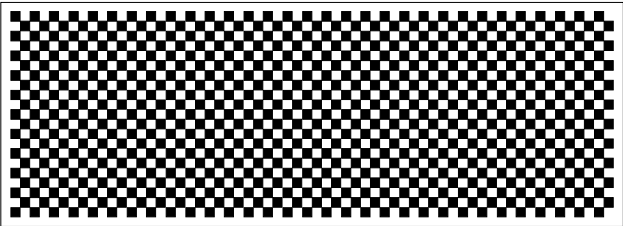
The test program displays the patterns in the following sequence. Every time when the Touch panel is pressed, the next pattern is displayed. When the Touch panel is pressed at the final pattern the display returns to the menu screen.

1) Liquid Crystal Display Check

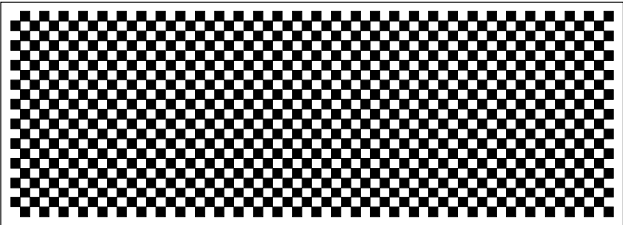
① Check content

The test patterns are displayed in the following sequence. When the Touch panel is pressed, the next pattern is displayed.

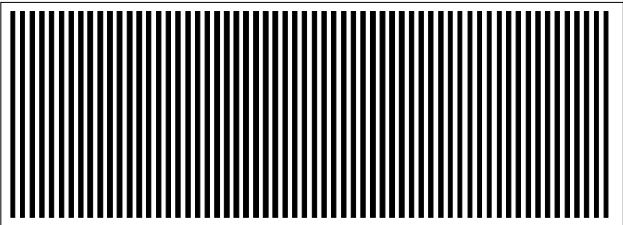
i. Black and white pattern at 1 dot pitch



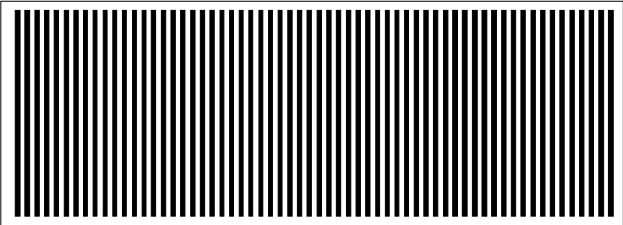
ii. Reversed pattern of the above (i)



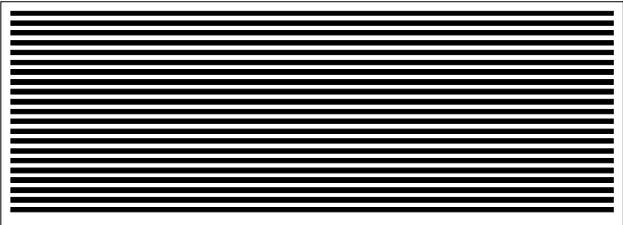
iii. Vertical stripe pattern at 1 dot pitch



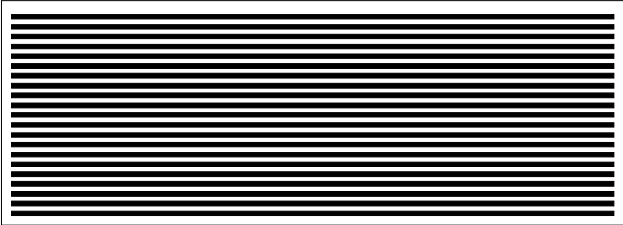
iv. Reversed pattern of the above (iii)



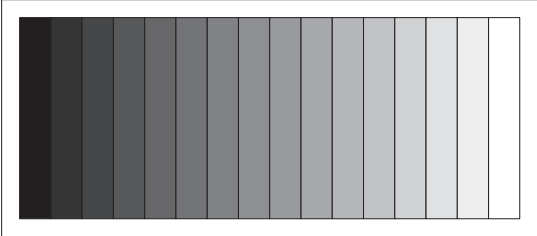
v. Horizontal stripe pattern at 1 dot pitch



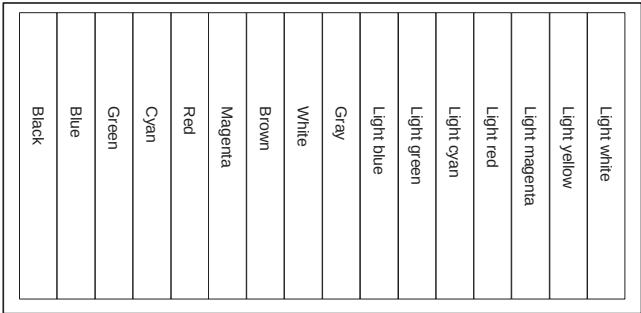
vi. Reversed pattern of the above (v)



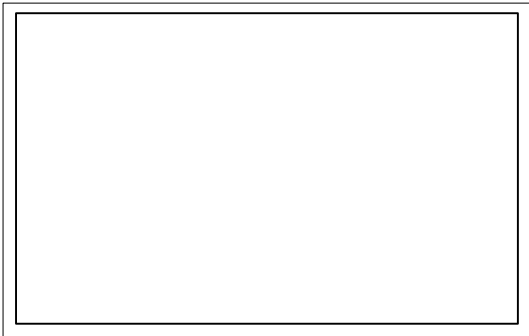
vii. Sixteen patterns of gradation ranging from black to white are displayed from left to right of the screen.



viii. 16-color bars are displayed.
from left: black, blue, green, cyan, red, magenta, brown, white, gray, light blue, light green, light cyan, light red, light magenta, light yellow, and light white

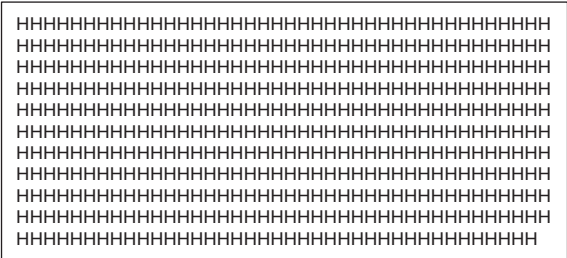


ix. The outermost peripheral of the LCD's active area is displayed in one-dot line.



White retester test

x. "H" pattern. "H" is displayed in 80 digits and 25 lines. The 15th line only has 39 digits of "H."



③ Terminating procedure
Press the Touch panel at the final pattern, or press the CANCEL key to terminate the check.

3-8. Rear Display Diagnostics

The rear display is checked.

The test program displays the following patterns. When the Touch panel is pressed, the display returns to the diagnostics menu.

1) Rear Display Check

① Check content

The test patterns are displayed in the following sequence. When the Touch panel is pressed, the next pattern is displayed.

i. The test pattern below is displayed.

ALPHA DISPLAY: 0 1 2 3 4 5 6 7 8 9 ; A a B b C

7-SEG DISPLAY: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, -;
 ▼ ▼ ▼ ▼ ▼ ▼ ▼ ▼ ▼ ▼ ▼

- ii. The test pattern with all the elements ON is displayed.

ALPHA DISPLAY:

7-SEG DISPLAY: 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8, 8,
 ▼ ▼ ▼ ▼ ▼ ▼ ▼ ▼ ▼ ▼ ▼ ▼

② Display

Rear Display Check

③ Terminating procedure

Press the Touch panel to turn off all the elements of the rear display.

3-9. SHARP Retail Network Diagnostics

The SRN test is performed.

To perform this test, the following composition is required.

- UP-3300
- Terminal resistor
- Branch (trunk) cable (only for data transfer test)

The following menu is displayed. Press the touch key for of the operation you want to execute to execute individual Diag programs.

Pressing the CANCEL key returns the screen to the Diag MAIN menu.

SRN Diagnostics	
Self Check	
Flag Check (need of SRV reset!)	
Data Check (need of SRV reset!)	
Data Check (Satellite Machine)	
Data Check (Master Machine)	
	Cancel

1) SRN Self Check

① Check content

The ROM and RAM for SRN are checked, and CTC interruption and carrier sense are checked. Also ADLC function and transmission/reception DMA check is made by using the self loop function of ADLC (MC6854). In addition, the other signals are checked. The check procedure is as follows:

- Execute diagnostics command 2. The number of resending is displayed.
- Execute diagnostics command 0. The error status is displayed. The error status is as shown in the table below. When an error occurs in this test, the following tests are not performed.

b7	An error occurs. (The error print is always 1.)
b6	An unexpected interruption is made.
b5	A collision is generated.
b4	An interruption of send complete cannot be made. (DMAC TC UP interruption)
b3	An interruption of carrier OFF cannot be made. The mirror image of carrier OFF shows carrier ON.
b2	An interruption of CTC CH2 or CH3 cannot be made. (Timer interruption)
b1	ROM sum check error
b0	TAM error

- Execute diagnostics command 1. The error status is displayed. The error status is as shown in the table below.

b7	An error is generated. (The error print is always 1.)
b6	An unexpected interruption is generated.
b5	DMA sent data and received data are different.
b4	The number of data received in DMA is abnormal.
b3	The number of data transmitted in DMA is abnormal.
b2	An overrun error is generated.
b1	An underrun error is generated.
b0	An interruption of send complete cannot be made. (DMAC TC UP interruption)

- Execute diagnostics command 5. The error status is displayed. The names and the directions of the signals which are subject to diagnostics 5 command are as shown in the table below.

Signal name	Direction
Power interruption notice	Host → Controller
Power interruption ON initialization	Host → Controller
Power interruption ON continuation	Host → Controller
Power interruption process complete	Host ← Controller
CH1 reception data present.	Host ← Controller
CH2 reception data present.	Host ← Controller

Check that the target bit of two statuses obtained by diagnostics 5 command is "0" for ST1 and "1" for ST2. (The other bits must be masked.) In the other cases, the error status is displayed with the error occurrence bit as "1." The normal bit shows "0."

The error status from the host to the controller is as shown in the table below.

b7	Not used. ("0" is always displayed.)
b6	Power interruption notice
b5	Not used. ("0" is always displayed.)
b4	Not used. ("0" is always displayed.)
b3	Not used. ("0" is always displayed.)
b2	Not used. ("0" is always displayed.)
b1	Power ON continuation
b0	Power ON initializing

The error status from the controller to the host is as shown in the table below.

b7	Not used. ("0" is always displayed.)
b6	Power interruption notice
b5	Not used. ("0" is always displayed.)
b4	CH2 reception data exits.
b3	CH1 reception data exits.
b2	Power interruption process complete
b1	Not used. ("0" is always displayed.)
b0	Not used. ("0" is always displayed.)

② Display

SRN Self Check

DATA RETRY CNT.=xxx	] The number of resending is displayed in xxx with a decimal number.
ACK RETRY CNT.=xxx	
DIAG 0 : xxxxxxxx	In the sequence of b7, b6, ..., b0 from the left. "1" is displayed in case of an error, and "0" when normal.
DIAG 1 : xxxxxxxx	In the sequence of b7, b6, ..., b0 from the left. "1" is displayed in case of an error, and "0" when normal.
DIAG 5 H→C : xxxxxxxx	In the sequence of b7, b6, ..., b0 from the left. "1" is displayed in case of an error, and "0" when normal.
DIAG 5 H←C : xxxxxxxx	In the sequence of b7, b6, ..., b0 from the left. "1" is displayed in case of an error, and "0" when normal.

③ Terminating procedure

Perform the service reset.

2) SRN Flag Send Check

① Check content

Execute diagnostics 3 command to send Flag (7EH) continuously.

② Display

SRN Flag Send Check

③ Terminating procedure

Perform the service reset.

3) SRN Data Send Check

① Check content

Execute diagnostics 4 command to send data of 00H~FFH (256Byte) as one packet at 12.8msec packet interval at 1Mbps continuously.

② Display

SRN Data Send Check

③ Terminating procedure

Perform the service reset.

4) Data Transmission Check

Data transmission is checked in an actually composed system. The system is composed of one master machine and max. 15 satellite machines.

Note for starting the check

- When checking the set in which the SRN setting has been made, cancel the SRN setting before starting this check.
- When checking the actually composed system, disconnect the SRN cables of the sets which are not checked, or cancel the SRN setting. If it is set to "SRN exits," data may be destroyed.
- The transmission check setting must be performed after canceling the SRN setting of all the sets in the system. First, set the satellite machines, then set the master machine.

① Setting procedure

• Satellite machine setting

In the menu screen, select "Data Transmission Check (Satellite)."

The display is as follows:

Data Transmission Check (Satellite)

Input Terminal Number :

Enter the terminal No. (000~015) of the machine to be checked and press the Touch panel. The display is as shown below.

Data Transmission Check (Satellite)

Input Terminal Number : xxx —The entered
Data Sequence Number : 0000 terminal No. is
displayed.

• Master machine setting

In the menu screen, select "Data Transmission Check (Master Machine)." The display is as shown below.

Data Transmission Check (Master)

Input Master Terminal Number :

Enter the terminal No. (000~015) of the machine to be checked and press the Touch panel. The display is as shown below.

Data Transmission Check (Master)

Input Master Terminal Number : xxx —The entered
Input Satellite Terminal Number: terminal No.
is displayed.

Enter the terminal No. (000~015) of the machine to be connected to the machine to be checked and press the ENTER key. The display is as shown below.

Data Transmission Check (Master)

Input Master Terminal Number : xxx
Input Satellite Terminal Number: xxx —The entered
terminal No. of satellite
machine is
displayed.

When checking with two or more satellite machines connected, enter the terminal No. (000 ~ 015) and press the ENTER key for each satellite connected. To execute, press the ENTER key without entering the terminal No. The display is as shown below. Do not use the same terminal No. for different machines (master/satellite).

```

Data Transmission Check (Master)

Input Master Terminal Number : xxx
Input Satellite Terminal Number : xxx
xxx xxx xxx xxx xxx

Data Sequence Number : 0000
  
```

With the above setting, data transmission between the master machine and the satellite machine is started.

② Check content

- Data in the following format composed of 2byte sequence No. and 254byte AAH data are transmitted from the master machine to the satellite machine. The master machine displays the sequence No.

Test data format (1 packet = 256byte)

1	2	3	4	5	...	...	...	254	255	256	Byte
XX	XX	AA	AA	AA	...	...	...	AA	AA	AA	

XXXX : Sequence No. (2byte: 4digits of binary decimal numbers)
AA : Transmission data (AAH) x 254 bytes

- The satellite machine sends back the received data to the master machine. The satellite machine displays the received sequence No.
- The master machine receives the data, and checks the sequence No. and 256byte AAH data. In case of an error, the master machine displays an error code and terminates the check. If two or more satellite machines are used, the above operation is repeated. If data transmission with all the satellite machines are normally completed, the master machine increments the sequence No.

The above operation is repeated.

③ Error display

```

Data Transmission Check (Master)

Input Master Terminal Number : xxx
Input Satellite Terminal Number : xxx
xxx xxx xxx xxx xxx

Data Sequence Number : xxxx
IRC Error : XX — The error code is displayed.
  
```

The error codes are as shown below.

01	Command abnormality (except for during transmission)
02	No data received.
03	Received data present. Received data remained.
04	Remote station not ready (in sending) "NTDY" is sent back because the remote station is not ready for reception.
05	Reception buffer full (in sending) The controller reception buffer of the remote machine is full.
06	Resend error (in sending) Retry over (5 times) when no response
07	Collision error (in sending) When an collision occurred in data transmission, retry over (16 times) at re-collision after a random time (0 ~ 255ms).
08	Line busy time out Transmission cannot be made by multi-station communication to cause time out in data send wait time.
09	Reception size over (in receiving) The reception buffer size is insufficient.
0A	Hardware error Interface abnormality (No SRN interface or abnormality in SRN controller)

③ Terminating procedure

Press the Touch panel to terminate the check.

3-10. IrDA & ASK Diagnostics

This is used to check the IR communication.

To execute this check, the following composition is required.

- UP-3300
- UP-3300 as checker

The following menu is displayed. Press the touch key for the operation you want to execute to execute individual Diag programs.

Pressing the CANCEL key returns the screen to the Diag MAIN menu.

```

IR(IrDA & ASK) Diagnostics

IrDA & ASK Check
IrDA & ASK Check(CHECKER MODE)
Data Check (Receive MODE)
Data Check (Send MODE)
IrDA, ASK & SRN Check(CHECKER)
Cancel
  
```

CAUTION: IrDA, ASK & SRN check (CHECKER) is used only in the production process, and must be not used in servicing.

1) IrDA & ASK Check

IR communication is checked between the UP-3300 sending unit and the receiving unit.

① Check content

- Data transmission is made from the machine to be checked in ASK format. The transmission rate is 9600bps. Data of 00H, 11H, 22H, 33H, 44H, 55H, 66H, 77H, 88H, 99H, AAH, BBH, CCH, EEH, and FFH are transmitted.
- The checker machine sends back the received data.
- The machine to be checked compares the data sent back and the data transmitted first. If both data are the same, it displays "PASS !," and if not the same, "ERROR !."
- Data transmission is made from the machine to be checked in IrDA format. The transmission rate is 9600bps. Data of 00H, 11H, 22H, 33H, 44H, 55H, 66H, 77H, 88H, 99H, AAH, BBH, CCH, EEH, and FFH are transmitted.
- The checker machine sends back the received data.
- The machine to be checked compares the data sent back and the data transmitted first. If both data are the same, it displays "PASS !," and if not the same, "ERROR !."

② Display

IrDA & ASK Check

ASK DATA (or TIMEOUT) : PASS!!(or ERROR!!)
IrDA DATA (or TIMEOUT) : PASS!!(or ERROR!!)

③ Terminating procedure

Press the Touch panel to terminate the check.

2) IrDA & ASK Check (checker mode)

Set the checker machine (UP-3300) corresponding to the above check content (1).

② Display

IrDA & ASK Check (CHECKER MODE)

ASK DATA (or TIMEOUT) : PASS!!(or ERROR!!)
IrDA DATA (or TIMEOUT) : PASS!!(or ERROR!!)

③ Terminating procedure

Press the Touch panel to terminate the check.

3) Data Transmission Check (Receive mode)

① Check content

Continuous IR communication between the UP-3300 and the UP-3300. This mode is on the reception side. When data of 256byte (00H ~ 0FFH) are received, the data packet counter is incremented by one. Check that the counter increments.

② Display

Data Transmission Check (Receive MODE)

COUNTER : **** (The RING COUNTER (0~9999) is displayed.)

③ Terminating procedure

Press the Touch panel to terminate the check.

4) Data Transmission Check (Send mode)

① Check content

Continuous IR communication between the UP-3300 and the UP-3300. This mode is on the transmission side. When data of 256byte (00H ~ 0FFH) are transmitted, the data packet counter is incremented by one. Check that the counter increments.

② Display

Data Transmission Check (Send MODE)

COUNTER : **** (The RING COUNTER (0~9999) is displayed.)

③ Terminating procedure

Press the Touch panel to terminate the check.

3-11. Magnetic Card Reader Diagnostics

Read check of the optional UP-E12MR2 is performed.

The test program reads the magnetic card of ISO 7811/1-5 standard and displays the data. When the Touch panel is pressed, the display returns to the diagnostics menu.

1) Magnetic Card Reader Check

① Check content

The test program reads tracks 1 and 2 of the magnetic card of ISO 7811/1-5, and displays the data in ASCII code.

② Display

MCR (Magnetic Card Reader) Check

TRACK1:

XX
XXXXXXXXXX

XX

TRACK2:

XX

XXXXXX shows the data read by the MCR. In case of an error, the error code is displayed as shown below.

Magnetic Card Reader Check

TRACK1:BUFFER EMPTY	—Displayed when TRACK1 empty code is sent back.
TRACK1:MCR ERROR	—Displayed when TRACK1 error code is sent back.
TRACK2:BUFFER EMPTY	—Displayed when TRACK2 empty code is sent back
TRACK2:MCR ERROR	—Displayed when TRACK2 error code is sent back.

③ Terminating procedure

Press the Touch panel to terminate the check.

3-12. Drawer Diagnostics

This diagnostics is used to check the drawer open and sensors.

The following menu is displayed. Press the position of the operation you want to execute to execute individual Diag programs.

Pressing the CANCEL key returns the screen to the Diag MAIN menu.

Drawer Diagnostics

Drawer 1 Check

Drawer 2 Check

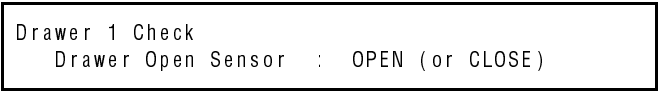
Cancel

1) Drawer 1 Check

① Check content

The solenoid of drawer 1 is turned on, and the drawer open sensor value is sensed at every 100ms, and the state is displayed.

② Display



③ Terminating procedure

Press the Touch panel to terminate the check.

2) Drawer 2 Check

① Check content

The solenoid of drawer 2 is turned on, and the drawer open sensor value is sensed at every 100ms, and the state is displayed.

The display and the terminating procedure are the same as Drawer 1 Check.

② Indication

The indication is the same as that for RS232 DIAGNOSTICS.

③ End

Press the PANEL to end the program.

2) Printer Print Check

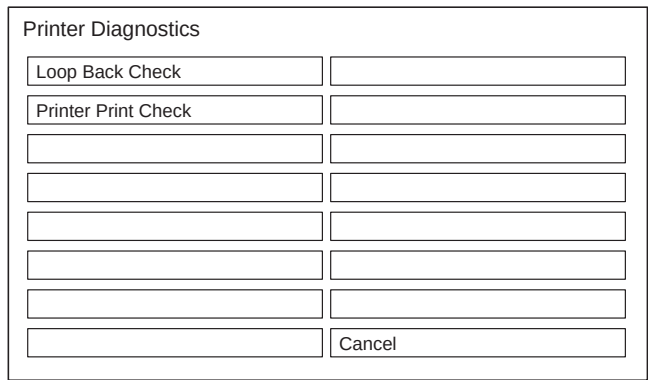
① Check

Send the signal to generate a receipt (by DIAG COMMAND) to the UP-T80BP.

3-13 Printer Diagnostics

I/F loopback and printing tests of the printer are performed.

The following menu appears. Press the name of the test you want to perform to execute its Diag program. When the Diag program is terminated, the screen returns to the Printer Diagnostics menu. Pressing the CANCEL key returns to screen to the Diag Menu.



1) Loop Back Check

① Check

A LOOPBACK test on the built-in printer (UP-T80BP) interface (logic channel 7 of RS232) is performed and the result is displayed. The test itself is the same as that for the RS232. The difference in test specifications is as follows: The loopback signals are for ER-DR, RS-CS, TXD-RXD only and the following LOOPBACK-Connectors are required.

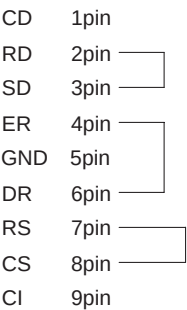


Fig.3-11. Wiring diagram of loopback connectors (UKOG-2356BHZZ)

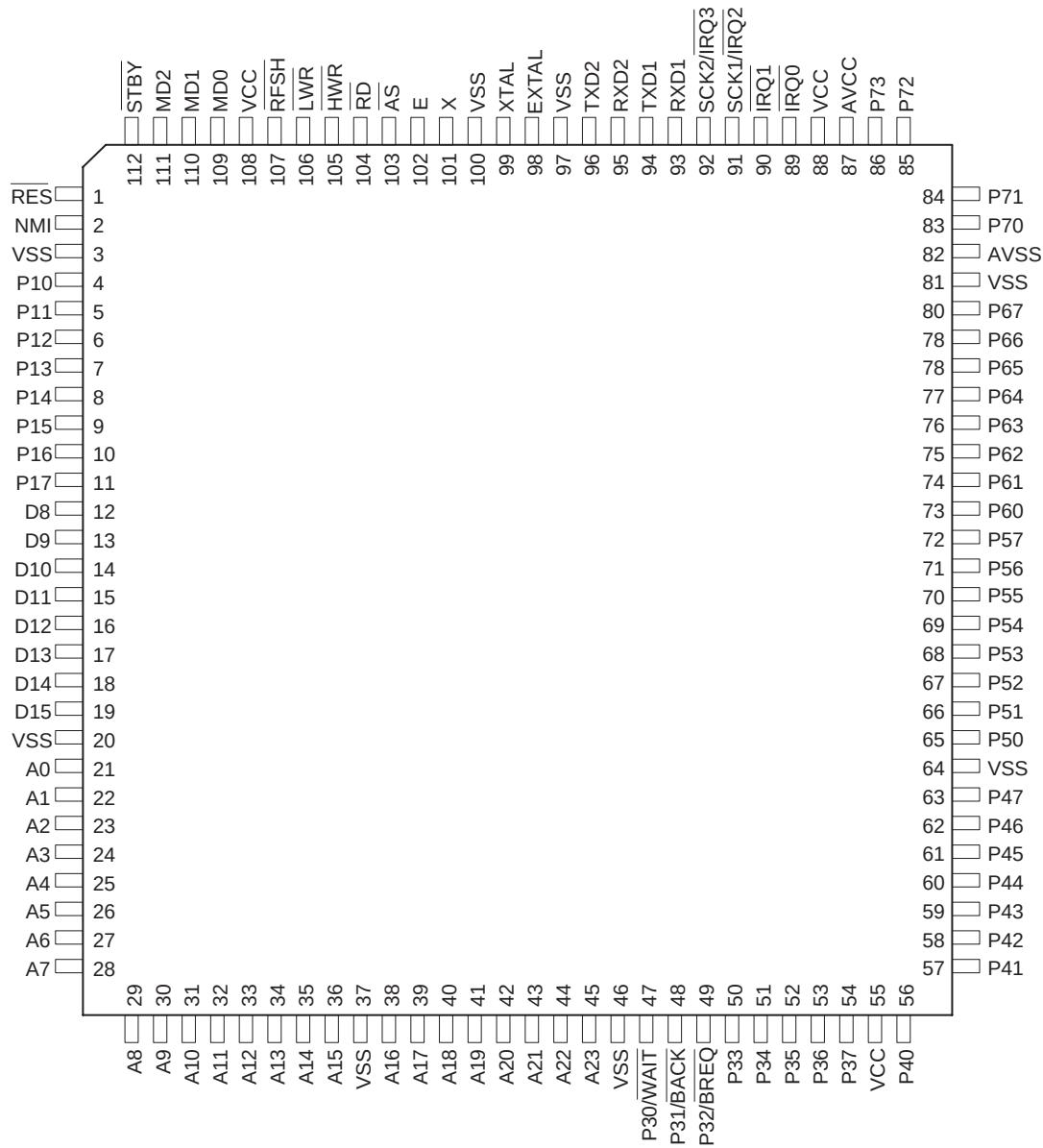
1. Hardware block diagram



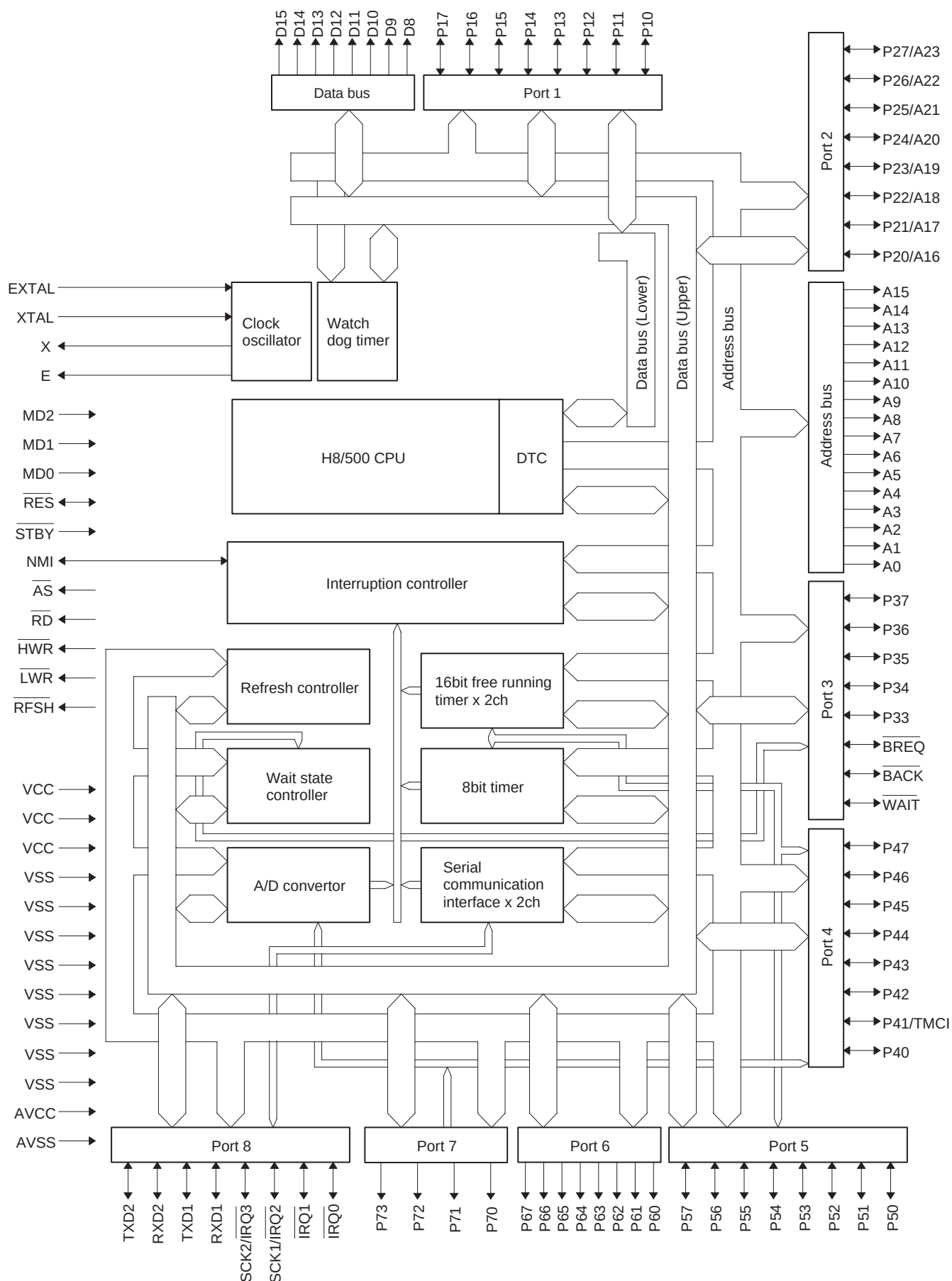
2. Description of main LSI's

2-1. CPU (HD6415108FX)

1) Pin description



2) Block diagram



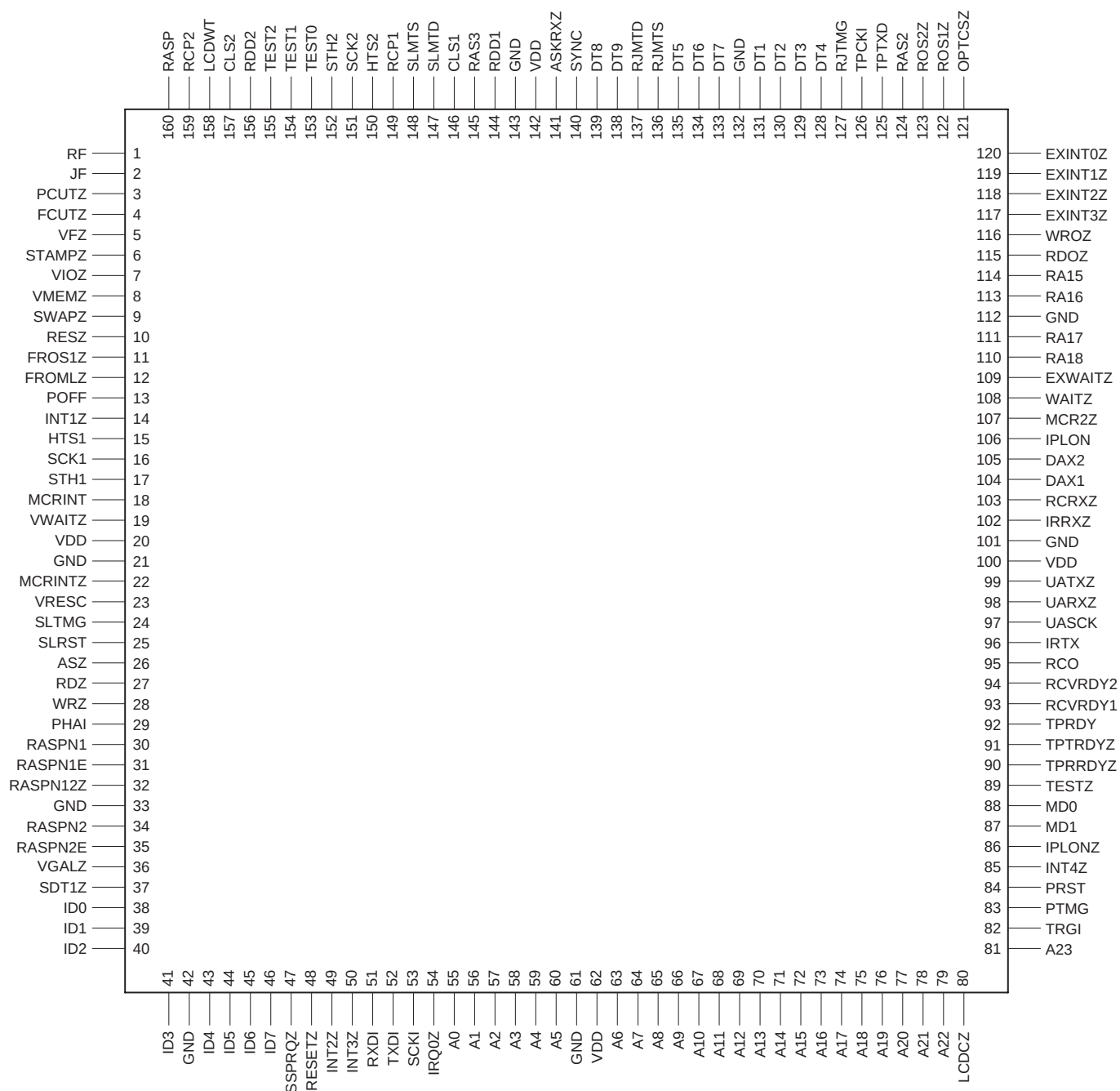
3) Pin description

Pin No.	Symbol	Signal name	In/ Out	Function
1	/RES	/RESET	In	Reset signal
2	NMI	NMI	In	Non-maskable interrupt input for SSP interrupt input.
3	VSS	GND	In	GND
4	D0	D0	I/O	Data bus
5	D1	D1	I/O	Data bus
6	D2	D2	I/O	Data bus
7	D3	D3	I/O	Data bus
8	D4	D4	I/O	Data bus
9	D5	D5	I/O	Data bus
10	D6	D6	I/O	Data bus
11	D7	D7	I/O	Data bus
12	D8	D8	I/O	Data bus
13	D9	D9	I/O	Data bus
14	D10	D10	I/O	Data bus
15	D11	D11	I/O	Data bus
16	D12	D12	I/O	Data bus
17	D13	D13	I/O	Data bus
18	D14	D14	I/O	Data bus
19	D15	D15	I/O	Data bus
20	VSS	GND	In	GND
21	A0	A0	Out	Address bus
22	A1	A1	Out	Address bus
23	A2	A2	Out	Address bus
24	A3	A3	Out	Address bus
25	A4	A4	Out	Address bus
26	A5	A5	Out	Address bus
27	A6	A6	Out	Address bus
28	A7	A7	Out	Address bus
29	A8	A8	Out	Address bus
30	A9	A9	Out	Address bus
31	A10	A10	Out	Address bus
32	A11	A11	Out	Address bus
33	A12	A12	Out	Address bus
34	A13	A13	Out	Address bus
35	A14	A14	Out	Address bus
36	A15	A15	Out	Address bus
37	VSS	GND	In	GND
38	A16	A16	Out	Address bus
39	A17	A17	Out	Address bus
40	A18	A18	Out	Address bus
41	A19	A19	Out	Address bus
42	A20	A20	Out	Address bus
43	A21	A21	Out	Address bus
44	A22	A22	Out	Address bus
45	A23	A23	Out	Address bus
46	VSS	GND	In	GND
47	P30	/WAIT	In	Wait signal
48	P31	/BACK	Out	Bus control request acknowledge signal
49	P32	/BREQ	In	Bus control request signal
50	P33	DOPS	In	Drawer open signal
51	P34	/DR0	Out	Option drawer open signal
52	P35	/DR1	Out	Option drawer open signal
53	P36	NC	NC	NC
54	P37	NC	NC	NC
55	VCC	VCC	In	+5V
56	P40	VCC	In	+5V
57	P41	GND	In	GND
58	P42	GND	In	GND

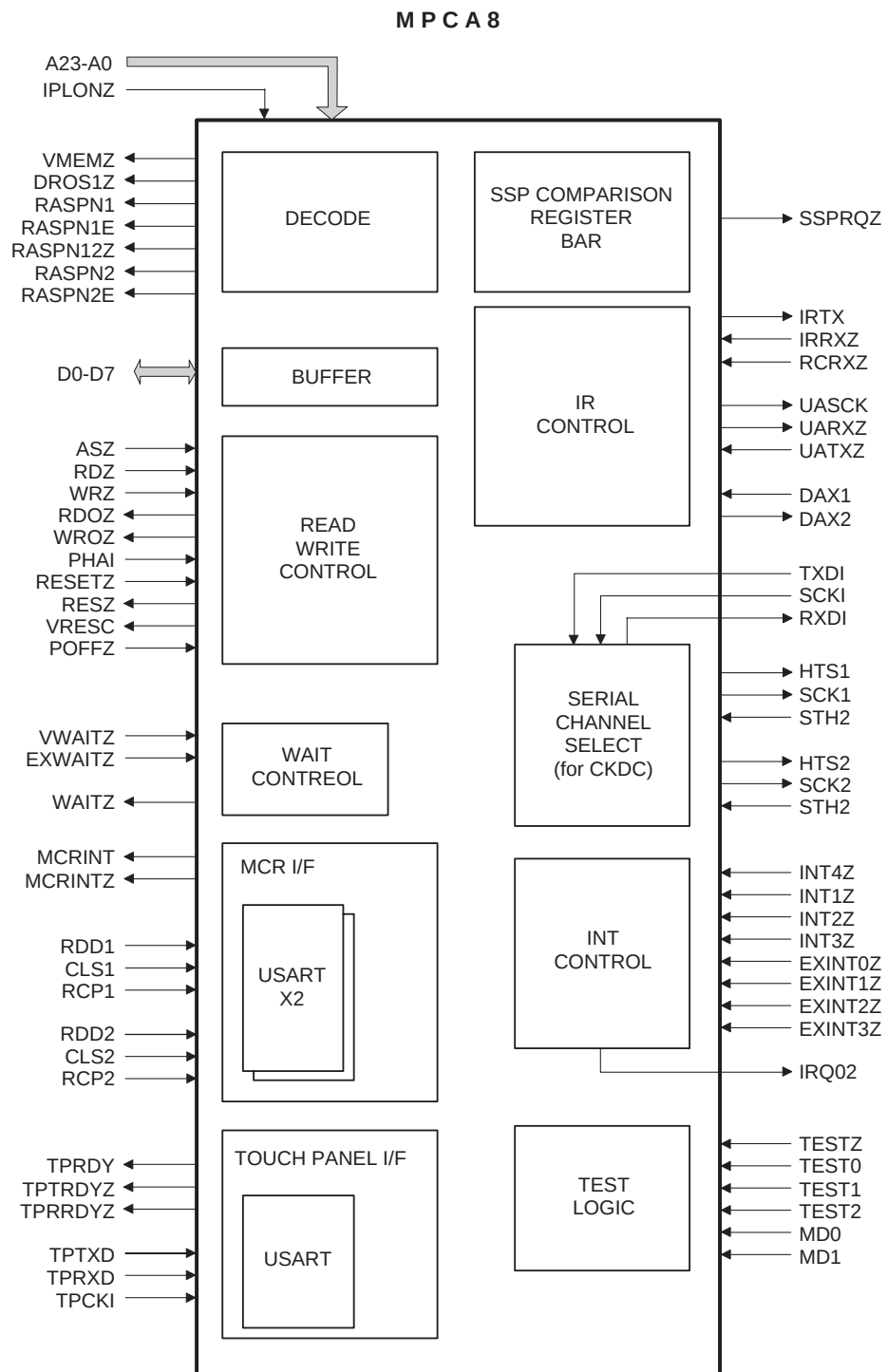
Pin No.	Symbol	Signal name	In/ Out	Function
59	P43	GND	In	GND
60	P44	MCRINT	In	MCR interrupt signal
61	P45	GND	In	GND
62	P46	/SHEN	In	CKDC interface shift enable signal
63	P47	GND	In	GND
64	VSS	GND	In	GND
65	P50	GND	In	GND
66	P51	GND	In	GND
67	P52	GND	In	GND
68	P53	GND	In	GND
69	P54	GND	In	GND
70	P55	GND	In	GND
71	P56	GND	In	GND
72	P57	/STOP	Out	System reset output signal
73	P60	/IPLON0	In	From IPL SW of ER-A7RS
74	P61	/IPLON1	In	From IPL SW of UP-3300
75	P62	GND	In	GND
76	P63	NORDY	In	Flash Memory ready ("H" active)
77	P64	FVPON	Out	Flash Memory write protect ("L" active)
78	P65	BANK	Out	For IPL ROM
79	P66	GND	In	GND
80	P67	GND	In	GND
81	VSS	GND	In	GND
82	AVSS	GND	In	GND
83	P70	GND	In	GND
84	P71	GND	In	GND
85	P72	GND	In	GND
86	P73	GND	In	GND
87	AVCC	VCC	In	+5V
88	VCC	VCC	In	+5V
89	/IRQ0	/IRQ0	In	Interrupt signal 0
90	/IRQ1	/IRQ1	In	Interrupt signal 1
91	/IRQ2	UASCK	In	Synchronizing shift clock signal for IR
92	/IRQ3	SCKI	Out	CKDC interface synchronizing shift clock
93	RXD1	/UARX	In	RXD signal for IR
94	TXD1	/UATX	Out	TXD signal for IR
95	RXD2	RXDI	In	CKDC interface shift input data
96	TXD2	TXDI	Out	CKDC interface shift output data
97	VSS	GND	In	GND
98	EXTAL	EXTAL	In	Crystal oscillator connection 19.6MHz
99	XTAL	XTAL	In	Crystal oscillator connection 19.6MHz
100	VSS	GND	In	GND
101	X	#	Out	System clock
102	E	NC	NC	NC
103	/AS	/AS	Out	Address strobe
104	RD	/RD	Out	Read signal
105	/HWR	/HWR	Out	Write signal (HIGH)
106	/LWR	/LWR	Out	Write signal (LOW)
107	/RFSH	/RFSH	Out	Refresh cycle signal
108	VCC	VCC	In	+5V
109	MD0	IPLON0	In	From IPL SW of ER-A7RS
110	MD1	IPLON0	In	From IPL SW of ER-A7RS
111	MD2	/IPLON0	In	From IPL SW of ER-A7RS
112	/STBY	VCC	In	+5V

2-2. G.A.(MPCA8)

1) Pin configuration



2) Block diagram



3) Pin description

Pin No.	Name	I/O	Description
1	RF	ON	NU
2	JF	ON	NU
3	PCUTZ	ON	NU
4	FCUTZ	ON	NU
5	VFZ	ON	NU
6	STAMPZ	ON	NU
7	VIOZ	O	NU
8	VMEMZ	O	VRAM DEOCDE
9	SWAPZ	O	NU
10	RESZ	O6M	RESET
11	FROS1Z	O	FLASH ROM DECODE
12	FROMLZ	O	NU
13	POFF	IC	POWER OFF SIGNAL INPUT
14	INT1Z	ICU	INTERRUPT SIGNAL INPUT
15	HTS1	O	SERIAL OUT (CKDC INTERFACE)
16	SCK1	O	SERIAL CLOCK (CKDC INTERFACE)
17	STH1	IS	SERIAL IN (CKDC INTERFACE)
18	MCRINT	O	MCR INTRRUPT OUT
19	VWAITZ	IU	VGA WAIT INPUT
20	VDD	–	
21	GND	–	
22	MCRINTZ	O	MCR INTRRUPT OUT
23	VRESC	ON	TURNS ACTIVE WHEN RESET&POWER DOWN IS MET
24	SLTMG	ICS	GND
25	SLRST	ICS	GND
26	ASZ	I	ADDRESS STROBE
27	RDZ	I	READ STROBE
28	WRZ	I	WRITE STROBE
29	PHAI	IS	SYSTEM CLOCK (9.83MHz)
30	RASPN1	O	PSRAM DECODE1
31	RASPN1E	O	PSRAM DECODE1 (EVEN)
32	RASPN12Z	O	PSRAM DECODE1 OR 2
33	GND	–	
34	RASPN2	O	PSRAM DECODE2
35	RASPN2E	O	PSRAM DECODE2(EVEN)
36	VGALZ	O	NU
37	SDT1Z	O	NU
38	ID0	IO	DATA BUS
39	ID1	IO	DATA BUS
40	ID2	IO	DATA BUS
41	ID3	IO	DATA BUS
42	GND	–	
43	ID4	IO	DATA BUS
44	ID5	IO	DATA BUS
45	ID6	IO	DATA BUS
46	ID7	IO	DATA BUS
47	SSPRQZ	O	SSP REQUEST FOR CPU
48	RESETZ	ICS	MPCA RESET
49	INT2Z	ICU	INTERRUPT INPUT (/TPRRDY)
50	INT3Z	ICU	INTERRUPT INPUT (/TPTRDY)

Pin No.	Name	I/O	Description
51	RXDI	O	SERIAL OUT FOR CPU
52	TXDI	IS	SERIAL IN FROM CPU
53	SCKI	IU	SERIAL CLOCK FROM CPU
54	IRQ0Z	O	INTERRUPT SIGNAL FOR CPU
55	A0	I	ADDRESS BUS
56	A1	I	ADDRESS BUS
57	A2	I	ADDRESS BUS
58	A3	I	ADDRESS BUS
59	A4	I	ADDRESS BUS
60	A5	I	ADDRESS BUS
61	GND	–	
62	VDD	–	
63	A6	I	ADDRESS BUS
64	A7	I	ADDRESS BUS
65	A8	I	ADDRESS BUS
66	A9	I	ADDRESS BUS
67	A10	I	ADDRESS BUS
68	A11	I	ADDRESS BUS
69	A12	I	ADDRESS BUS
70	A13	I	ADDRESS BUS
71	A14	I	ADDRESS BUS
72	A15	I	ADDRESS BUS
73	A16	I	ADDRESS BUS
74	A17	I	ADDRESS BUS
75	A18	I	ADDRESS BUS
76	A19	I	ADDRESS BUS
77	A20	I	ADDRESS BUS
78	A21	I	ADDRESS BUS
79	A22	I	ADDRESS BUS
80	LCDCZ	O	NU
81	A23	I	ADDRESS BUS
82	TRGI	IS	NU
83	PTMG	O	NU
84	PRST	O	NU
85	INT4Z	ICU	NU
86	IPLONZ	IU	IPL SIGNAL FROM OPTION CONNECTER
87	MD1	ICU	TEST PIN
88	MD0	ICU	TEST PIN
89	TESTZ	ICU	TEST PIN
90	TPRRDYZ	O	TOUCH PANEL INTERRUPT (CONNECTED TO INT2Z)
91	TPTRDYZ	O	TOUCH PANEL INTERRUPT (CONNECTED TO INT3Z)
92	TPRDY	O	NU
93	RCVRDY1	IU	NU
94	RCVRDY2	IU	NU
95	RCO	O	NU
96	IRTX	O	IR OUT
97	UASCK	O	IR CLOCK
98	UARXZ	O	IR DATA FOR CPU
99	UATXZ	IU	IR DATA FROM CPU

Pin No.	Name	I/O	Description
100	VDD	–	
101	GND	–	
102	IRRXZ	ICS	IR IN FROM IR UNIT
103	RCRXZ	ICS	NU
104	DAX1	OSCI	IR CLOCK (7.37MHz)
105	DAX2	OSCO	IR CLOCK (7.37MHz)
106	IPLON	O	IPLON SIGNAL
107	MCR2Z	O	NU
108	WAITZ	O	WAIT FOR CPU
109	EXWAITZ	IU	EXTERNAL WAIT INPUT SIGNAL
110	RA18	O	NU
111	RA17	O	NU
112	GND	–	
113	RA16	O	NU
114	RA15	O	NU
115	RDOZ	O8M	EXPANSION RD
116	WROZ	O8M	EXPANSION WR
117	EXINT3Z	ICS	EXPANSION INTERRUPT SIGNAL
118	EXINT2Z	ICS	EXPANSION INTERRUPT SIGNAL
119	EXINT1Z	ICS	EXPANSION INTERRUPT SIGNAL
120	EXINT0Z	ICS	EXPANSION INTERRUPT SIGNAL
121	OPTCSZ	O	BASE DECODE SIGNAL FOR EXPANSION SLOT
122	ROS1Z	O	NU
123	ROS2Z	O	NU
124	RAS2	O	NU
125	TPTXD	O	SERIAL OUT FOR TOUCH PANEL
126	TPRXD	ICS	SERIAL IN FROM TOUCH PANEL
127	TPCKI	ICS	SERIAL CLOCK 9.83MHz/64 (TOUCH PANEL INTERFACE)
128	DT4	ON	NU
129	DT3	ON	NU
130	DT2	ON	NU
131	DT1	ON	NU
132	GND	–	
133	DT7	ON	NU
134	DT6	ON	NU
135	DT5	ON	NU
136	RJMTS	ON	NU
137	RJMTD	ON	NU
138	DT9	ON	NU
139	DT8	ON	NU
140	SYNC	IU	NU
141	ASKRXZ	ICS	IR INPUT FROM IR UNIT
142	VDD	–	
143	GND	–	
144	RDD1	ICS	SERIAL IN FROM MCR TRACK1
145	RAS3	O	NU
146	CLS1	ICS	CARD SENSE ON MCR TRACK1
147	SLMTD	ON	NU
148	SLMTS	ON	NU
149	RCP1	ICS	CLOCK PULSE FROM MCR TRACK1

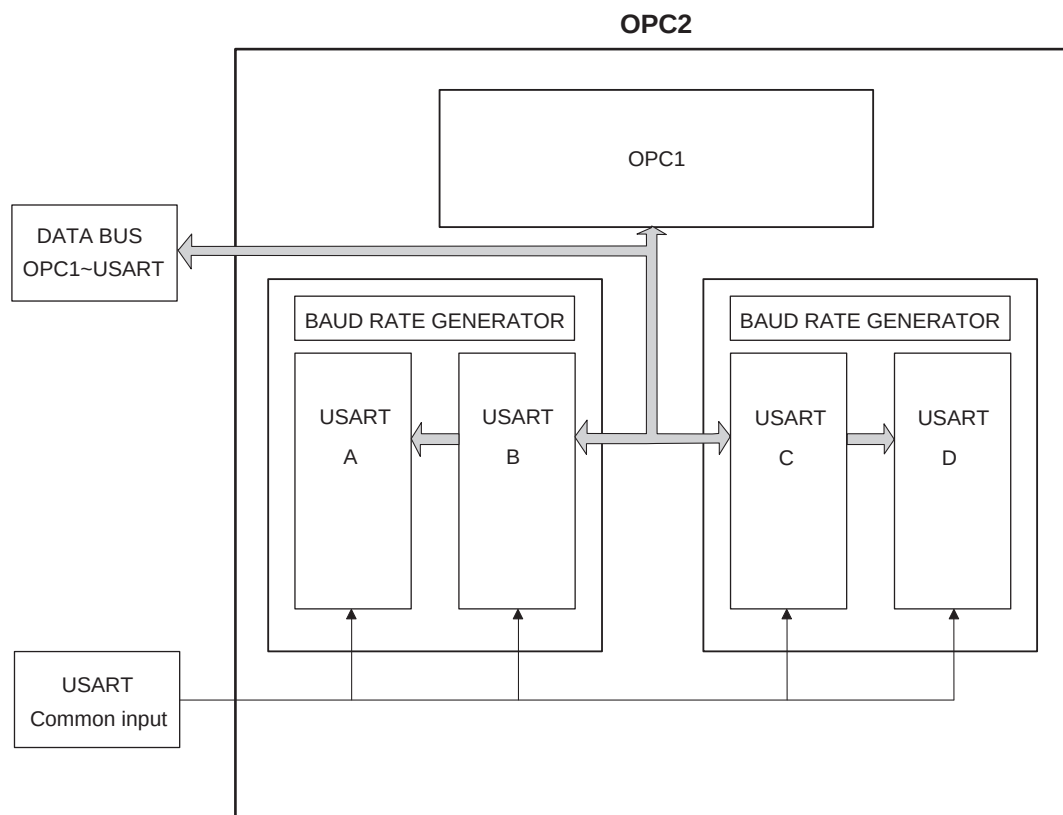
Pin No.	Name	I/O	Description
150	HTS2	O	SERIAL OUT (OPTION CKDC INTERFACE) NU
151	SCK2	O	SERIAL CLOCK (OPTION CKDC INTERFACE) NU
152	STH2	IS	SERIAL IN (OPTION CKDC INTERFACE) NU
153	TEST0	I	TEST PIN
154	TEST1	I	TEST PIN
155	TEST2	I	TEST PIN
156	RDD2	ICS	SERIAL IN FROM MCR TRACK1
157	CLS2	ICS	CARD SENSE ON MCR TRACK1
158	LCDWT	IU	NU
159	RCP2	ICS	CLOCK PULSE FROM MCR TRACK1
160	RASP	O	NU

I TTL input
 IS TTL Schmitt input
 IU TTL pull up input
 IC CMOS input
 ICS CMOS Schmitt input
 ICU CMOS pull up input
 IO TTL I/O
 O Output 4mA
 O8M Output 8mA
 ON Nch open drain output
 OSIC Oscillation circuit input
 OSCI Oscillation circuit output

1) Pin configuration



2) Block diagram



3) Pin description

Pin NO.	Name	UP-3300	I/O	Description
1	SL00	VCC	ISU	RS-232/UNIT0 channel select
2	SL01	GND	ISU	
3	SL02	GND	ISU	
4	SL10	GND	ISU	RS-232/UNIT1 channel select
5	SL11	VCC	ISU	
6	SL12	GND	ISU	
7	SL20	VCC	ISU	RS-232/UNIT2 channel select
8	SL21	VCC	ISU	
9	SL22	VCC	ISU	
10	SL30	GND	ISU	RS-232/UNIT3 channel select
11	SL31	GND	ISU	
12	SL32	GND	ISU	
13	/CD0	/DCD1	IS	RS-232 control signal /CD input
14	BRK0	BRK1	IS	RS-232 break signal
15	TRNEMP0	TRENMP1	IS	RS-232 transmission buffer empty signal
16	RCVRDY0	RCVRDY1	IS	RS-232 data reception enable signal
17	TRNRDY0	TRNRDY1	IS	RS-232 transmission enable signal
18	/CTS0	/CTS1	IS	RS-232 clear to send signal
19	RCVDT0	RCVDT1	IS	RS-232 reception data signal
20	VCC	VCC		+5V
21	GND	GND		GND
22	/CI0	/CI1	IS	RS-232 control signal /CI input
23	/RTS0	/RTS1	O	RS-232 request to send signal

Pin NO.	Name	UP-3300	I/O	Description
24	/CS0	/CS1	O	RS-232 chip select signal
25	/CD1	/DCD2	IS	RS-232 control signal /CD input
26	BRK1	BRK2	IS	RS-232 break signal
27	TRNEMP1	TRENMP2	IS	RS-232 transmission buffer empty signal
28	RCVRDY1	RCVRDY2	IS	RS-232 data reception enable signal
29	TRNRDY1	TRNRDY2	IS	RS-232 transmission enable signal
30	/CTS1	/CTS2	IS	RS-232 clear to send signal
31	RCVDT1	RCVDT2	IS	RS-232 reception data signal
32	/CI1	/CI2	IS	RS-232 control signal /CI input
33	/RTS1	/RTS2	O	RS-232 request to send signal
34	/CS1	/CS2	O	RS-232 chip select signal
35	/CD2	VCC	IS	+5V
36	TRNEMP2	TRENMP3	IS	RS-232 transmission buffer empty signal
37	RCVRDY2	RCVRDY3	IS	RS-232 data reception enable signal
38	TRNRDY2	TRNRDY3	IS	RS-232 transmission enable signal
39	CTS2Z	/CTS3	IS	RS-232 clear to send signal

Pin NO.	Name	UP-3300	I/O	Description
40	RCVDT2	RCVDT3	IS	RS-232 reception to send signal
41	/CI2	VCC	IS	+5V
42	/CS2	/CS3	O	RS-232 chip select signal
43	/CD3	/SINT	IS	RS-232: /CD, IN-LINE : /P1
44	BRK3	GND	IS	GND
45	TRNEMP3	GND	IS	GND
46	RCVRDY3	GND	IS	GND
47	TRNRDY3	GND	IS	GND
48	/CTS3	GND	IS	GND
49	RCVDT3	GND	IS	GND
50	/CI3	GND	IS	GND
51	/CS3	/SRCS	O	RS-232/INLINE chip select signal
52	D0	D0	IO	Data bus (CPU)
53	D1	D1	IO	Data bus (CPU)
54	D2	D2	IO	Data bus (CPU)
55	D3	D3	IO	Data bus (CPU)
56	GND	GND		GND
57	D4	D4	IO	Data bus (CPU)
58	D5	D5	IO	Data bus (CPU)
59	D6	D6	IO	Data bus (CPU)
60	D7	D7	IO	Data bus (CPU)
61	GND	GND		GND
62	VCC	VCC		+5V
63	X1	NC	O OSI14	NC
64	X2	#	I OSI14	System clock
65	XOUT	CLK_USART	O	Clock (USART)
66	TRCK	NC	O	NC
67	AB0	AH0	O	Address bus for USART
68	AB1	AH1	O	Address bus for USART
69	US1CH	GND	IS	GND
70	PX	NC	O	NC
71	/POF	/POFF	IS	POFF signal
72	/RSRQ	/IRQ1	3S	RS232 INTRRUPT
73	/TRV	GND	IS	GND
74	RXDATA0	NC	O	NC
75	TXE	/SRESET	O	INLINE TRNS ENABLE
76	/TRRQ	/TRQ2	3S	INLINE INTRRUPT
77	/TRQ1	/TRQ1	ON6	TIMER INTRRUPT (RS232)
78	/TRQ2	NC	ON6	TIMER INTRRUPT (INLINE)
79	A0	A0	I	Address bus for CPU
80	A1	A1	I	Address bus for CPU
81	A2	A2	I	Address bus for CPU
82	A3	A3	I	Address bus for CPU
83	A4	A4	I	Address bus for CPU
84	A5	A5	I	Address bus for CPU
85	/OPTCS	/OPTCS	I	Option chip select (from MPCA)
86	/RD	/RDO	I	Read signal (from CPU)
87	/WR	/WRO	I	Write signal (from CPU)
88	/RES	/RES	IS	Reset signal (from CPU)
89	DB0	DB0	IO	DATA BUS (USART)

Pin NO.	Name	UP-3300	I/O	Description
90	DB1	DB1	IO	DATA BUS (USART)
91	DB2	DB2	IO	DATA BUS (USART)
92	DB3	DB3	IO	DATA BUS (USART)
93	GND	GND		GND
94	DB4	DB4	IO	DATA BUS (USART)
95	DB5	DB5	IO	DATA BUS (USART)
96	DB6	DB6	IO	DATA BUS (USART)
97	DB7	DB7	IO	DATA BUS (USART)
98	/R	/RDH	O	Read signal (to USART)
99	/W	/WRH	O	Write signal (to USART)
100	VCC	VCC		+5V
101	GND	GND		GND
102	RES	RES USART	O	Reset signal (to USART)
103	TRNCLK	GND	I	GND
104	RCVCLK	GND	I	GND
105	DBTST	/SRCS	ID	RS-232/INLINE USART chip select
106	UTST	VCC	ID	+5V
107	/CSA	/CS1	IS	USART_A chip select
108	TRNDTA	TXD1	O	RS-232 transmission data signal
109	/DTRA	/DTR1	O	RS-232 data terminal ready signal
110	/RTSA	NC	O	NC
111	RCVDTA	RCVDT1	IS	RS-232 reception data signal
112	/CTSA	GND	IS	GND
113	/DSRA	/DSR1	IS	RS-232 data set ready signal
114	TRNRDYA	TRNRDY1	O	RS-232 data transmission enable signal
115	RCVRDYA	RCVRDY1	O	RS-232 data reception enable signal
116	TRNEMPA	TRNEMP1	O	RS-232 transmission buffer empty signal
117	SYCBKA	BRK1	IO	Break code detection signal
118	GND	GND		GND
119	/CSB	/CS2	IS	USART_B chip select
120	TRNDTB	TXD2	O	RS-232 transmission data signal
121	/DTRB	/DTR2	O	RS-232 data terminal ready signal
122	/RTSB	NC	O	NC
123	RCVDTB	RCVDT2	IS	RS-232 reception data signal
124	/CTSB	GND	IS	GND
125	/DSRB	/DSR2	IS	RS-232 data set ready signal
126	TRNRDYB	TRNRDY2	O	RS-232 data transmission enable signal
127	RCVRDYB	RCVRDY2	O	RS-232 data reception enable signal
128	TRNEMPB	TRNEMP2	O	RS-232 transmission buffer empty signal
129	SYCBKB	BRK2	IO	Break code detection signal
130	GND	GND		GND

Pin NO.	Name	UP-3300	I/O	Description
131	/CSC	/CS3	IS	USART_C chip select
132	TRNDTC	TXD3	O	RS-232 transmission data signal
133	/DTRC	/DTR3	O	RS-232 data terminal ready signal
134	/RTSC	/RTS3	O	USART_C request to send
135	RCVDTC	RCVD3	IS	RS-232 reception data signal
136	/CTSC	GND	IS	GND
137	/DSRC	/DSR3	IS	RS-232 data set ready signal
138	TRNRDYC	TRNRDY3	O	RS-232 data transmission enable signal
139	RCVRDYC	RCVRDY3	O	RS-232 data reception enable signal
140	TRNEMPC	TRNEMP3	O	RS-232 transmission buffer empty signal
141	SYCBKC	NC	IO	NC
142	VCC	VCC		+5V
143	GND	GND		GND
144	/CSD	VCC	IS	USART_D chip select
145	TRNDTD	NC	O	NC
146	/DTRD	NC	O	NC
147	/RTSD	NC	O	NC
148	RCVDTD	GND	IS	GND
149	/CTSD	GND	IS	GND
150	/DSRD	GND	IS	GND
151	TRNRDYD	NC	O	NC
152	RCVRDYD	NC	O	NC
153	TRNEMPD	NC	O	NC
154	SYCBKD	NC	IO	NC
155	/WIN	/WRH	I	Write signal
156	/RIN	/RDH	I	Read signal
157	RSLCT0	AH0	I	Address bus
158	RSLCT1	AH1	I	Address bus
159	RST	RES USART	IS	Reset signal
160	MCLK	CLK USART	I	

I	TTL input
ID	TTL input with pull down
IS	TTL Schmidt input
ISU	TTL Schmidt input with pull up
IO	TTL I/O
3S	3-state Buffer (6mA)
ON6	Open drain (6mA)

2-4. Z80 CPU

1) Features

The extensive instruction set contains 158 instructions, including the 8080A instruction set as a subset.

- NMOS version for low cost high performance solutions, CMOS version for high performance low power designs.
- Z0840006 - 6.17 MHz
- CMOS Z84C0006 - DC to 6.17 MHz, Z84C008 - DC to 8 MHz, Z84C0010 - DC to 10 MHz, Z84C0020 - DC - 20 MHz
- 6 MHz version can be operated at 6.144 MHz clock.

- The Z80 microprocessors and associated family of peripherals can be linked by a vectored interrupt system. This system can be daisy-chained to allow implementation of a priority interrupt scheme.
- Duplicate set of both general-purpose and flag registers.
- Two sixteen-bit index registers.
- Three modes of maskable interrupts:
Mode 0 — 8080A similar;
Mode 1 — Non-Z80 environment, location 38H;
Mode 2 — Z80 family peripherals, vectored interrupts.
- On-chip dynamic memory refresh counter.

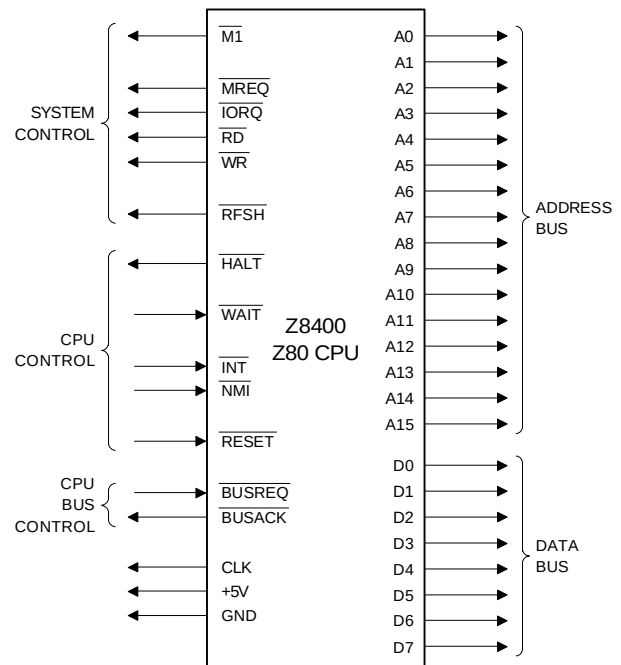
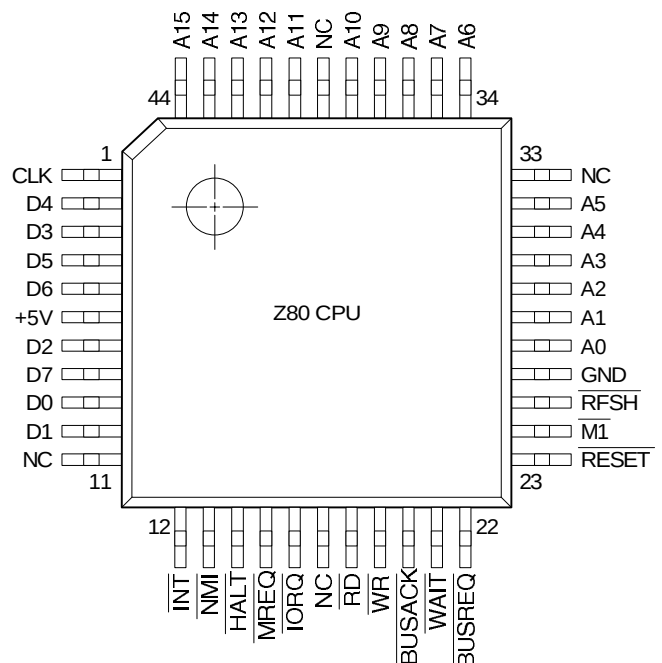


Figure 1. Pin functions

2) Pin configuration



44 pin Quad Flat Pack (QFP), Pin Assignments
(Only available for 84C00)

3) General description

The CPUs are fourth-generation enhanced microprocessors with exceptional computational power. They offer higher system throughput and more efficient memory utilization than comparable second- and third-generation microprocessors. The internal registers contain 208 bits of read/write memory that are accessible to the programmer.

These registers include two sets of six general-purpose registers which may be used individually as either 8-bit registers or as 16-bit register pairs. In addition, there are two sets of accumulator and flag registers. A group of "Exchange" instructions makes either set of main or alternate registers accessible to the programmer. The alternate set allows operation in foreground-background mode or it may be reserved for very fast interrupt response.

The CPU also contains a Stack Pointer, Program Counter, two index registers, a Refresh register (counter), and an Interrupt register. The CPU is easy to incorporate into a system since it requires only a single +5V power source. All output signals are fully decoded and timed to control standard memory or peripheral circuits; the CPU is supported by an extensive family of peripheral controllers.

The internal block diagram (Figure 3) shows the primary functions of the processors. Subsequent text provides more detail on the I/O controller family, registers, instruction set, interrupts and daisy chaining, and CPU timing.

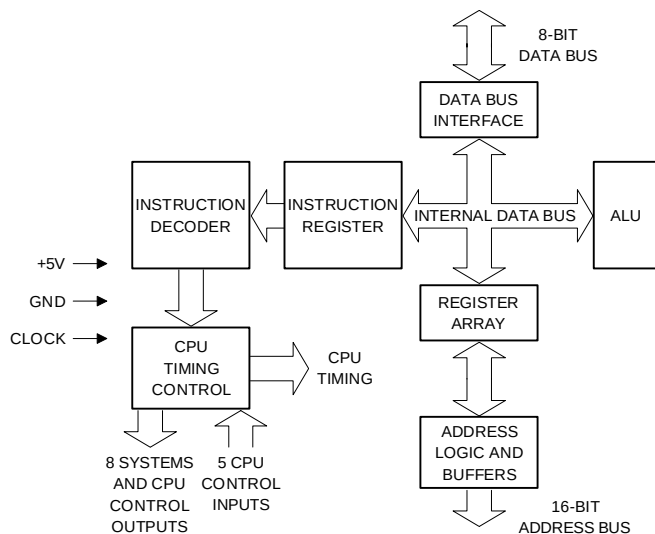


Figure 3. Z80C CPU Block Diagram

4) Pin description

Pin No.	Symbol	Signal name	In/Out	Function
1	CLK	CLK	In	Clock
2	D4	S D4	In/Out	Data bus
3	D3	S D3	In/Out	Data bus
4	D5	S D5	In/Out	Data bus
5	D6	S D6	In/Out	Data bus
6	+5V	VCC	—	+5V
7	D2	S D2	In/Out	Data bus
8	D7	S D7	In/Out	Data bus
9	D0	S D0	In/Out	Data bus
10	D1	S D1	In/Out	Data bus
11	NC	NC	—	NC
12	$\overline{\text{INT}}$	S INT	In	Interrupt request signal
13	$\overline{\text{NMI}}$	VCC	—	Non-maskable interrupt signal
14	$\overline{\text{HALT}}$	VCC	—	+5V
15	$\overline{\text{MREQ}}$	S $\overline{\text{MRQ}}$	Out	Memory request signal
16	$\overline{\text{IORQ}}$	S $\overline{\text{IORQ}}$	Out	Input / Output request signal
17	NC	NC	—	NC

Pin No.	Symbol	Signal name	In/Out	Function
18	$\overline{\text{RD}}$	S $\overline{\text{RDS}}$	Out	Rread signal
19	$\overline{\text{WR}}$	S $\overline{\text{WRS}}$	Out	Write signal
20	$\overline{\text{BUSAK}}$	$\overline{\text{BUSAK}}$	Out	Bus acknowledge signal
21	$\overline{\text{WAIT}}$	S $\overline{\text{WAIT}}$	In	Wait signal
22	$\overline{\text{BUSRQ}}$	$\overline{\text{BUSRQ}}$	In	Bus request signal
23	$\overline{\text{RESET}}$	S $\overline{\text{RES}}$	In	Reset signal
24	$\overline{\text{M1}}$	S M1	Out	Machine cycle one signal
25	$\overline{\text{RFSH}}$	NC	—	NC
26	GND	GND	—	GND
27	A0	S A0	Out	Address bus
28	A1	S A1	Out	Address bus
29	A2	S A2	Out	Address bus
30	A3	S A3	Out	Address bus
31	A4	S A4	Out	Address bus
32	A5	S A5	Out	Address bus
33	NC	NC	—	NC
34	A6	S A6	Out	Address bus
35	A7	S A7	Out	Address bus
36	A8	S A8	Out	Address bus
37	A9	S A9	Out	Address bus
38	A10	S A10	Out	Address bus
39	NC	NC	—	NC
40	A11	S A11	Out	Address bus
41	A12	S A12	Out	Address bus
42	A13	S A13	Out	Address bus
43	A14	S A14	Out	Address bus
44	A15	S A15	Out	Address bus

2-5. Z80 CTC

1) Features

- Four independently programmable counter/timer channels, each with a readable downcounter and a selectable 16 or 256 prescaler. Downcounters are reloaded automatically at zero count.
- Selectable positive or negative trigger initiates timer operation.
- Three channels have Zero Count/Timeout outputs capable of driving Darlington transistors. (1.5mV @ 1.5V)
- NMOS version for cost sensitive performance solutions.
- CMOS version for the designs requiring low power consumption
- NMOS Z0843004 - 4 MHz, Z0843006 - 6.17 MHz.
- CMOS Z84C3006 - DC to 6.17 MHz, Z84C3008 - DC to 8 MHz, Z84C3010 - DC to 10 MHz
- Interfaces directly to the Z80 CPU or—for baud rate generation—to the Z80 SIO.
- Standard Z80 Family daisy-chain interrupt structure provides fully vectored, prioritized interrupts without external logic. The CTC may also be used as an interrupt controller.
- 6 MHz version supports 6.144 MHz CPU clock operation.

2) General description

The Z80 CTC, hereinafter referred to as Z80 CTC or CTC, four-channel counter/timer can be programmed by system software for a broad range of counting and timing applications. The four independently programmable channels of the Z80 CTC satisfy common microcomputer system requirements for event counting, interrupt and interval timing, and general clock rate generation.

System design is simplified because the CTC connects directly to both the Z80 CPU and the Z80 SIO with no additional logic. In larger systems, address decoders and buffers may be required.

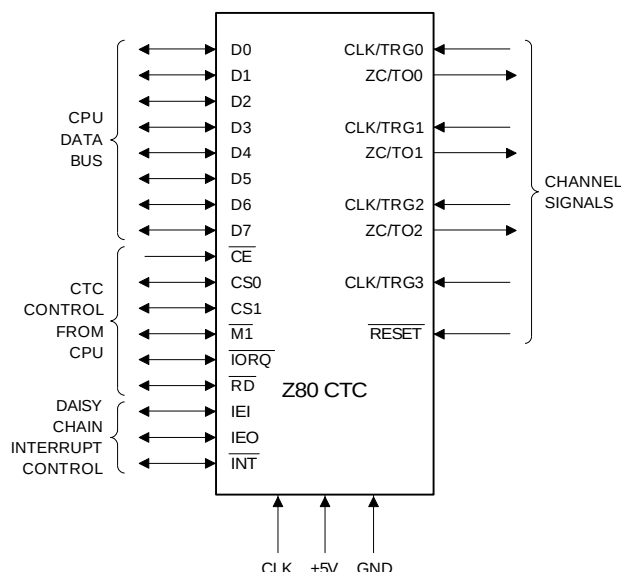


Figure 1. Pin Functions

Programming the CTC is straightforward: each channel is programmed with two bytes: a third is necessary when interrupts are enabled. Once started, the CTC counts down, automatically reloads its time constant, and resumes counting. Software timing loops are completely eliminated. Interrupt processing is simplified because only one vector need be specified: the CTC internally generates a unique vector for each channel.

The Z80 CTC requires a single +5% V power supply and the standard Z80 single-phase system clock. It is packaged in 28-pin DIPs, a 44-pin plastic chip carrier, and a 44-pin Quad Flat Pack. (Figures 2a, 2b, and 2c). Note that the QFP package is only available for CMOS versions.

3) Pin configuration

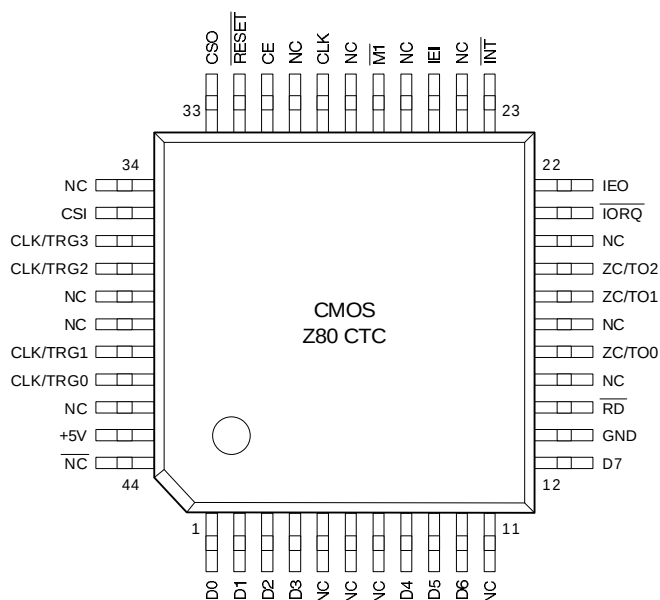


Figure 2c. 44-pin Quad Flat Pack Pin Assignments

4) Functional description

The Z80 CTC has four independent counter/timer channels. Each channel is individually programmed with two words: a control word and a time-constant word. The control word selects the operating mode (counter or timer), enables or disables the channel interrupt, and selects certain other operating parameters. If the timing mode is selected, the control word also sets a prescaler, which divides the system clock by either 16 or 256. The time-constant word is a value from 1 to 256.

During operation, the individual counter channel counts down from the preset time constant value. In counter mode operation the counter decrements on each of the CLK/TRG input pulses until zero count is reached. Each decrement is synchronized by the system clock. For counts greater than 256, more than one counter can be cascaded. At zero count, the down-counter is automatically reset with the time constant value.

The timer mode determines time intervals as small as 2 μ s (8 MHz), 3 μ s (6 MHz), or 4 μ s (4 MHz) without additional logic or software timing loops. Time intervals are generated by dividing the system clock with a prescaler that decrements a preset down-counter.

Thus, the time interval is an integral multiple of the clock period, the prescaler value (16 or 256), and the time constant that is preset in the down-counter. A timer is triggered automatically when its time constant value is programmed, or by an external CLK/TRG input.

Three channels have two outputs that occur at zero count.

The first output is a zero-count/timeout pulse at the ZC/TO output. The fourth channel (Channel 3) does not have a ZC/TO output; interrupt request is the only output available from Channel 3.

The second output is Interrupt Request (INT), which occurs if the channel has its interrupt enabled during programming. When the Z80 CPU acknowledges Interrupt Request, the Z80 CTC places an interrupt vector on the data bus.

The four channels of the Z80 CTC are fully prioritized and fit into four contiguous slots in a standard Z80 daisy-chain interrupt structure. Channel 0 is the highest priority and Channel 3 the lowest. Interrupts can be individually enabled (or disabled) for each of the four channels.

5) Pin description

Pin No.	Symbol	Signal name	In/Out	Function
1	D0	S D0	In/Out	Data bus
2	D1	S D1	In/Out	Data bus
3	D2	S D2	In/Out	Data bus
4	D3	S D3	In/Out	Data bus
5	NC	NC	—	NC
6	NC	NC	—	NC
7	NC	NC	—	NC
8	D4	S D4	In/Out	Data bus
9	D5	S D5	In/Out	Data bus
10	D6	S D6	In/Out	Data bus
11	NC	NC	—	NC
12	D7	S D7	In/Out	Data bus
13	GND	GND	—	GND
14	$\overline{RD}$	S $\overline{RDS}$	In	Read cycle status signal
15	NC	NC	—	NC
16	ZC/TO0	S TM0	Out	Zero count / Timeout signal
17	NC	NC	—	NC
18	ZC/TO1	NC	—	NC
19	ZC/TO2	NC	—	NC
20	NC	NC	—	NC
21	$\overline{IORQ}$	S IORQ	In	Input / Output request signal
22	IEO	NC	—	NC
23	$\overline{INT}$	S INT	Out	Interrupt request signal
24	NC	NC	—	NC
25	IEI	VCC	—	+5V
26	NC	NC	—	NC
27	$\overline{M1}$	S M1	In	Machine cycle one signal
28	NC	NC	—	NC
29	CLK	CLK	In	System clock
30	NC	NC	—	NC
31	$\overline{CE}$	S A6	In	Chip enable signal
32	$\overline{RESET}$	S $\overline{RES}$	In	Reset signal
33	CS0	S A0	In	Channelselect signal

Pin No.	Symbol	Signal name	In/Out	Function
34	NC	NC	—	NC
35	CS1	S A1	In	Channelselect signal
36	CLK/TRG3	S TM1	In	External clock / timer signal
37	CLK/TRG2	S TM0	In	External clock / timer signal
38	NC	NC	—	NC
39	NC	NC	—	NC
40	CLK/TRG1	S INTS	In	External clock / timer signal
41	CLK/TRG0	VCC	In	+5V
42	NC	NC	—	NC
43	+5V	VCC	—	+5V
44	NC	NC	—	NC

2-6. μ PD71037

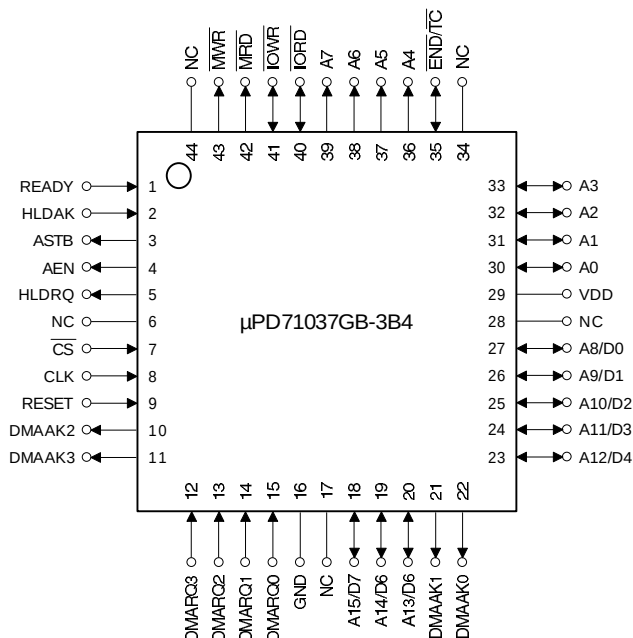
DMA CONTROLLER

The μ PD71037 is a direct memory access controller (DMAC) for the micro processor system. It provides higher processing speed and lower power consumption in comparison with those in conventional use. Each of the four built-in DMA channels has 64-KB addresses and the function of counting the number of bytes of transferred data, and can transfer data from I/O to memory and from memory to memory as well.

1) FEATURES

- The clock speed is 10 MHz, twice that of the μ PD8237A-5 (clock speed of 5 MHz).
- Each of the four DMA channels can be operated independently.
- Each channel can be self-initialized.
- Data is transferrable from memory to memory.
- Data in memory can independently initialized by block.
- High speed data transfer:
3.2 MB/sec. (clock seed of 10 MHz, normal transfer mode)
5.0 MB/sec. (clock speed of 10 MHz, compression transfer mode)
- The number of DMA channels can directly be expanded (Expansion mode).
- $\overline{\text{END}}$ input when data transfer is finished.
- Software DMA request available.
- CMOS
- Low power consumption

2) Pin configuration



2-7. MB62H149

1) Outline

The MB62H149 is a semi-custom LSI chip for the peripheral circuits in the SRN (SHARP Retail Network), its main function is to communicate data with the host CPU and control the peripheral circuits and transmission control circuits of the Sub CPU (Z-80). Fig. 2. shows the general configuration of the functions:

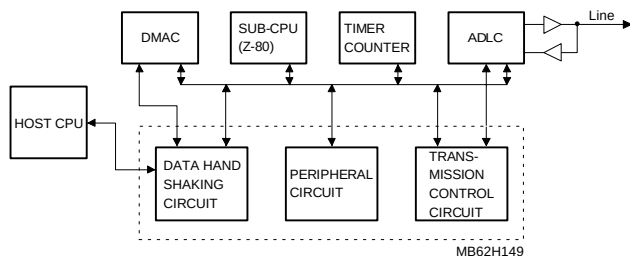


Fig. 2

2) Internal functions

(1) Data handshaking circuit

Is used because data processing speeds vary and the timing of the HOST CPU and SUB CPU do not synchronize, the MB62H149 is used for data handshaking. When the data handshaking portion is broken down, the system consists of a Write Signal from the HOST CPU to the MB62H149, Read Signal from the MB62H149 of the SUB CPU, Write Signal from the SUB CPU to the MB62H149 and Read Signal from the MB62H149 of the HOST CPU, all of which from two blocks as shown.

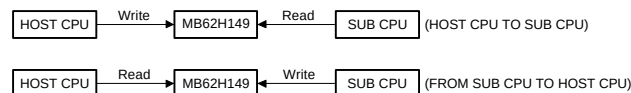


Fig. 3

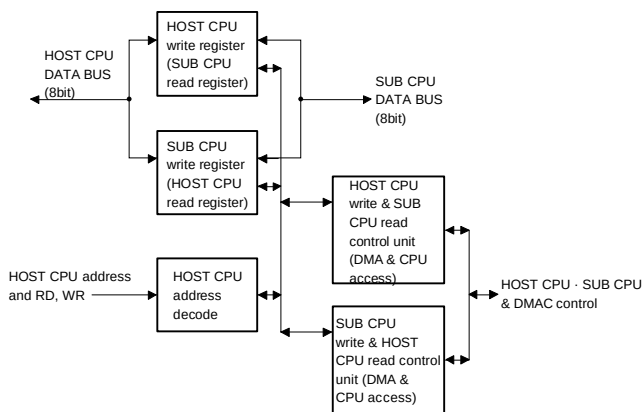


Fig. 4

(2) Peripheral circuit

The peripheral circuit consists of an I/O address generation unit on the SUB CPU, block dividing circuit, and the wait signal control unit.

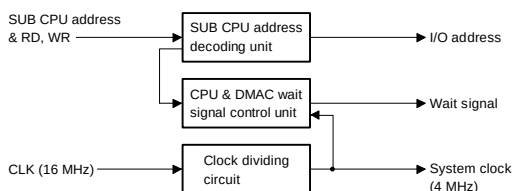


Fig. 5

(a) I/O address generation circuit

A total of 11 I/O addresses are generated by A0, A1, A4, A5 and RD and WR signals.

(b) CPU and DMAC wait signal control unit

Clocks into the CPU (Z-80), SUB CPU and its peripheral LSI, DMAC and CTC are operated respectively on 4 MHz.

While, the ADLC (MC68B54) (Advanced Data Link Control) is operated by the E (Enable clock) of 2 MHz according to restrictions in terms of the hardware of the LSI.

It is necessary to synchronize the timing of the write and read in the ADLC.

To control synchronization, timing, and input, the wait signal goes into the CPU for CPU access and into the DMAC for DMA access. This block is a circuit to generate such wait signal.

(c) Clock dividing circuit

This block divides the blocks according to the CLK supplied from outside to generate the clock for CPU, DMAC and CTC and the E and transmission clock rate (480 KBPS or 1 MBPS selectable) for the ADLC.

(3) Transmission control circuit

The transmission control circuit is divided into the modem unit, carrier detect unit, collision detect unit.

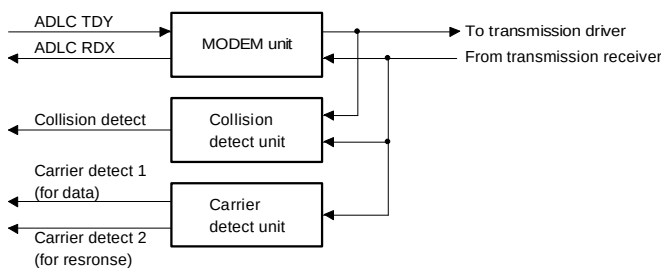


Fig. 6

(a) Modem circuit

The transmission data input from the ADLC are PE modulated (phase encoding modulation), the circuit to be output to the transmission driver and the reception data input from the transmission receiver are demodulated and produced at the ADLC.

(b) Collision detect circuit

The data transmitted from the home station is received and detects a collision on the transmission line by means of an exclusive OR gate.

(c) Carrier detect circuit

This circuit detects whether data is flowing on the transmission line. It consists of a circuit which immediately senses a no data status on the line. When data is not on the line the circuit functions to sense an elapse of the fixed time rate. The immediate sensing circuit is used for response testing and the delayed sensing circuit is used for data testing.

The fixed time rate is selectable according to the transmission speed as shown below via SRV-mode programming. Job #922.

Transmission speed	Delay time
1 MBPS	1.6m sec, 3.2m sec, 4.8m sec, 6.4m sec.
480 KBPS	3.2m sec, 6.4m sec, 9.6m sec, 12.8m sec.

3) Terminal Name and Description (MB62H149)

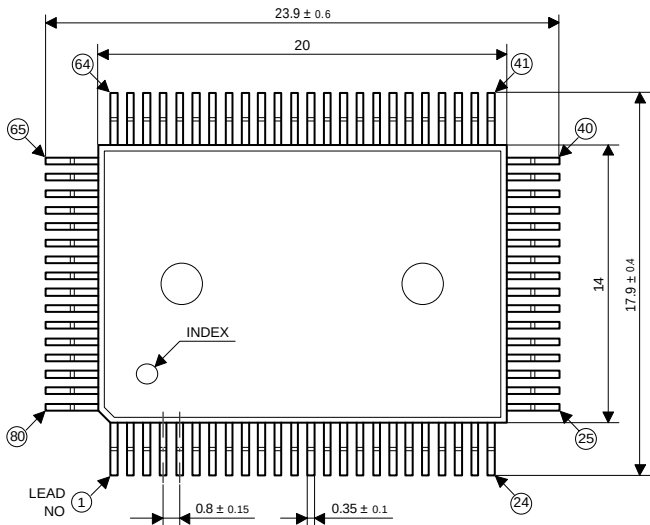


Fig. 7

Pin No.	Terminal name	Host/ Sub	In/ Out	Description
1	CLK	Sub	In	Clock in (16 MHz)
2	—	—	—	N.U.
3	$\overline{\text{IORQ}}$	Sub	In	I/O request
4	$\overline{\text{MREQ}}$	Sub	In	Memory request
5	$\overline{\text{RDS}}$	Sub	In	Read from sub
6	$\overline{\text{WRS}}$	Sub	In	Write from sub
7	$\overline{\text{INTS}}$	Sub	Out	Interrupt to sub
8	ϕ	Sub	Out	Clock out
9	TM0	Sub	In	Timer 0
10	TM1	Sub	Out	Timer 1
11	$\overline{\text{MRD}}$	Sub	Out	Memory read
12	VSS	—	—	GND
13	$\overline{\text{WAIT}}$	Sub	Out	Wait signal
14	A15	Sub	Out	Address bus for DMA
16	A9	Sub	Out	
17	A8	Sub	Out	
18	A5	Sub	In	
19	A4	Sub	In	
20	A1	Sub	In	
21	A0	Sub	In	
22	DAK01	Sub	In	
23	—	—	—	
24	$\overline{\text{MWR0}}$	Sub	Out	Memory write
25	D7	Sub	I/O	Data bus
26	D6	Sub	I/O	
27	D5	Sub	I/O	
28	D4	Sub	I/O	
29	D3	Sub	I/O	
30	D2	Sub	I/O	
31	D1	Sub	I/O	
32	D0	Sub	I/O	
33	VDD	—	—	+5V
34	—	—	—	N.U.
35	$\overline{\text{RES}}$	Host	In	Reset

Pin No.	Terminal name	Host/ Sub	In/ Out	Description
36	$\overline{\text{IO/WR}}$	Sub	I/O	I/O write
37	$\overline{\text{IO/RD}}$	Sub	I/O	I/O read
38	AEN	Sub	In	Address enable from DMAC
39	AST	Sub	In	Address strobe from DMAC
40	TCS	Sub	In	Terminal count
41	DAK23	Sub	In	DMA acknowledge 2+3
42	$\overline{\text{DRQRS}}$	Sub	Out	DMA request read to sub
43	$\overline{\text{DRQWS}}$	Sub	Out	DMA request write to sub
44	$\overline{\text{RDH}}$	Host	In	Read from Host
45	$\overline{\text{WRH}}$	Host	In	write from Host
46	$\overline{\text{INTH}}$	Host	Out	Interrupt to host
47	$\overline{\text{DAK}}$	Host	In	DMA acknowledge from host
48	TCH	Host	In	Terminal count from host
49	$\overline{\text{DRQWH}}$	Host	Out	DMA request read to host
50	$\overline{\text{DRQWH}}$	Host	Out	DMA request write to host
51	$\overline{\text{CS}}$	Host	In	Chip select from host
52	VSS	—	—	GND
53	—	—	—	N.U.
54	DB0	Host	I/O	Data bus
55	DB1	Host	I/O	
56	DB2	Host	I/O	
57	DB3	Host	I/O	
58	DB4	Host	I/O	
59	DB5	Host	I/O	
60	DB6	Host	I/O	
61	DB7	Host	I/O	Data bus
62	AB0	Host	In	
63	—	—	—	N.U.
64	AB1	Host	In	Address bus from host
65	COL	Sub	In	Collision detect signal
66	RDI	Sub	In	Receive data from receiver
67	TDI	Sub	Out	Transmmit data to driver
68	$\overline{\text{RTS}}$	Sub	In	Request to send
69	RXC	Sub	Out	Receive clock to ADLC
70	RXD	Sub	Out	Receive data to ADLC
71	TXC	Sub	Out	Transmmit clock
72	TXD	Sub	In	Transmmit data
73	VDD	—	—	+5V
74	E	Sub	In	Enable clock to ADLC
75	$\overline{\text{IRQ}}$	Sub	In	Interrupt request from ADLC
76	$\overline{\text{LCS}}$	Sub	Out	Link controller chip select
77	—	—	—	N.U.
78	RS1	Sub	Out	Register select 1
79	RS0	Sub	Out	Register select 0
80	MSK	Sub	Out	Mask signal

1) Pin Configuration



3) Pin configuration

Pin No.	Symbol	Signal name	In/ Out	Function
1	XIN	XIN	In	25.175MHz
2	GND	GND	In	GND
3	AEN	GND	In	GND
4	/SBEH	/SBEH	In	System byte high enable
5	/IOWR	/IOWR	In	I/O write
6	/IORD	/IORD	In	I/O read
7	/SMEMW	/SMEMW	In	Memory write
8	/SMEMR	/SMEMR	In	Memory read
9	A21	GND	In	GND
10	A20	GND	In	GND
11	SA19	VCC	In	+5V
12	SA18	GND	In	GND
13	SA17	VCC	In	+5V
14	SA16	A16	In	Address bus
15	SA15	A15	In	Address bus
16	SA14	A14	In	Address bus
17	SA13	A13	In	Address bus
18	SA12	A12	In	Address bus
19	SA11	A11	In	Address bus
20	SA10	A10	In	Address bus
21	SA9	A9	In	Address bus
22	SA8	A8	In	Address bus
23	SA7	A7	In	Address bus
24	SA6	A6	In	Address bus
25	SA5	A5	In	Address bus
26	SA4	A4	In	Address bus
27	SA3	A3	In	Address bus
28	SA2	A2	In	Address bus
29	SA1	A1	In	Address bus
30	SA0	A0	In	Address bus
31	/BIOWEN	NC	In	NC
32	/REFRESH	/RFSH	In	Refresh signal
33	GND	GND	In	GND
34	VDD	VCC	In	+5V
35	SD15	D7	I/O	Data bus
36	SD14	D6	I/O	Data bus
37	SD13	D5	I/O	Data bus
38	SD12	D4	I/O	Data bus
39	GND	GND	In	GND
40	SD11	D3	I/O	Data bus
41	SD10	D2	I/O	Data bus
42	SD9	D1	I/O	Data bus
43	VDD	VCC	In	+5V
44	SD8	D0	I/O	Data bus
45	SD7	D15	I/O	Data bus
46	SD6	D14	I/O	Data bus
47	GND	GND	In	GND
48	SD5	D13	I/O	Data bus
49	SD4	D12	I/O	Data bus
50	SD3	D11	I/O	Data bus
51	SD2	D10	I/O	Data bus
52	SD1	D9	I/O	Data bus
53	SD0	D8	I/O	Data bus
54	GND	GND	In	GND
55	VDD	VCC	In	+5V
56	IOCHRDY	/VWAITI	Out	Channel ready signal
57	/MEMCS16	NC	In	NC
58	/IOCS16	NC	In	NC
59	GND	GND	In	GND

Pin No.	Symbol	Signal name	In/ Out	Function
60	VDD	VCC	In	+5V
61	DCLK	XCK	Out	Data shift clock
62	DISP	DISP	Out	Display enable
63	LP	LP	Out	Line pulse
64	FP	YD	Out	Frame pulse
65	UD7	DU7	Out	Upper data
66	UD6	DU6	Out	Upper data
67	UD5	DU5	Out	Upper data
68	UD4	DU4	Out	Upper data
69	UD3	DU3	Out	Upper data
70	UD2	DU2	Out	Upper data
71	UD1	DU1	Out	Upper data
72	UD0	DU0	Out	Upper data
73	GND	GND	In	GND
74	VDD	VCC	In	+5V
75	LD7	DL7	Out	Lower data
76	LD6	DL6	Out	Lower data
77	LD5	DL5	Out	Lower data
78	LD4	DL4	Out	Lower data
79	LD3	DL3	Out	Lower data
80	LD2	DL2	Out	Lower data
81	LD1	DL1	Out	Lower data
82	LD0	DL0	Out	Lower data
83	BACKON	BKLT	Out	Back light On
84	LCDON	LCDON	Out	LCD drive power on signal
85	LOGICON	NC	Out	LCD logic power on signal
86	GND	GND	In	GND
87	VDD	VCC	In	+5V
88	MA9	NC	Out	NC
89	MA8	MA8	Out	Memory address bus
90	MA7	MA7	Out	Memory address bus
91	MA6	MA6	Out	Memory address bus
92	MA5	MA5	Out	Memory address bus
93	MA4	MA4	Out	Memory address bus
94	MA3	MA3	Out	Memory address bus
95	MA2	MA2	Out	Memory address bus
96	MA1	MA1	Out	Memory address bus
97	MA0	MA0	Out	Memory address bus
98	GND	GND	In	GND
99	VDD	VCC	In	VCC
100	/RAS	/RASV	Out	RAS address strobe
101	/UCAS	/UCASV	Out	Upper CAS address strobe
102	/LCAS	/LCASV	Out	Lower CAS address strobe
103	/WE	/WEV	Out	Write enable
104	MD15	MD15	I/O	Memory data
105	MD14	MD14	I/O	Memory data
106	MD13	MD13	I/O	Memory data
107	MD12	MD12	I/O	Memory data
108	MD11	MD11	I/O	Memory data
109	MD10	MD10	I/O	Memory data
110	GND	GND	In	GND
111	VDD	VCC	In	+5V
112	MD9	MD9	I/O	Memory data
113	MD8	MD8	I/O	Memory data
114	MD7	MD7	I/O	Memory data

Pin No.	Symbol	Signal name	In/ Out	Function
115	MD6	MD6	I/O	Memory data
116	MD5	MD5	I/O	Memory data
117	MD4	MD4	I/O	Memory data
118	MD3	MD3	I/O	Memory data
119	MD2	MD2	I/O	Memory data
120	MD1	MD1	I/O	Memory data
121	MD0	MD0	I/O	Memory data
122	GND	GND	In	GND
123	VDD	VCC	In	+5V
124	RESET	RESET	In	Reset signal
125	MINTEST	GND	In	GND
126	TEST	GND	In	GND
127	GND	GND	In	GND
128	XO	XO	Out	25.175MHz

2-9. CKDC9 (HD404728A91FS)

1) General description

The CKDC7 is a 4-bit microcomputer developed for the UP-3300 and provides functions to control the real-time clock, keys, and displays. The basic functions of the CKDC7 are shown below.

- Keys:** The CKDC9 is capable of controlling a maximum of 256 momentary keys. (Sharp 2-key rollover control)
Simultaneous scanning of key and switch
(When a key is scanned, the state of a mode and clerk switch is also buffered. The host can scan the state of switch together with the key entry data at the same time the key is scanned.)
- Switches:** Mode switch with 14 positions maximum
8-bit clerk (cashier) switch
2-bit feed switch
1-bit receipt on/off switch
1-bit option switch
4-bit general-purpose switch (1-bit is used for keyboard select)
- Displays:** 16-column dot display
12-column 7-segment display (column digit selectable)
All column blink controlled for the dot and 7-segment display decimal point and indicators
Programmable patterns for 7-segment display:
Four patterns
Internal driver for 7-segment display
- Buzzer:** Single tone control
- Clock:** Year, month, day of month, day of week, hour, minute
- Alarm:** Hour, minute
- Interrupt request (event control):**
Detection of key input, switch position change, alarm issue, and counter overflow

2) Pin description

Pin No.	Symbol	Signal name	In/ Out	Function
1	SB	SB	Out	Segment B
2	SC	SC	Out	Segment C
3	SD	SD	Out	Segment D
4	SE	SE	Out	Segment E
5	SF	SF	Out	Segment F
6	SG	SG	Out	Segment G
7	P4	AP	Out	
8	P0	NC	—	NC
9	P1	NC	—	NC
10	P2	DP	Out	Decimal point
11	P3	ID	Out	Indicator

Pin No.	Symbol	Signal name	In/ Out	Function
12	$\overline{\text{MODR}}$	VCC	—	+5V
13	$\overline{\text{CFSR}}$	$\overline{\text{CFSR}}$	In	Clerk key, Feed key, Switch return signal
14	KEX0	NC	Out	NC
15	KEX1	NC	Out	NC
16	RQ	GND	—	GND
17	SKR0	VCC	—	+5V
18	ST0	ST0	Out	Key strobe signal
19	ST1	ST1	Out	Key strobe signal
20	ST2	ST2	Out	Key strobe signal
21	ST3	ST3	Out	Key strobe signal
22	POFF	POFF	In	Power off signal
23	$\overline{\text{STOP}}$	$\overline{\text{STOP}}$	In	STOP signal
24	$\overline{\text{DDIG}}$	VCC	—	+5V
25	$\overline{\text{DCS}}$	$\overline{\text{DCS}}$	—	Dot display controller chip select DCS
26	VCC	$\overline{\text{VCKDC}}$	—	+5V
27	$\overline{\text{SCK}}$	$\overline{\text{SCK}}$	In	Clock signal
28	HTS	HTS	In	Key data from host
29	STH	STH	Out	Key data to host
30	SDISP	GND	—	GND
31	BUZZ	BUZZ	Out	Buzzer
32	$\overline{\text{DSCK}}$	$\overline{\text{DSCK}}$	—	Dot display controller $\overline{\text{SCK}}$
33	$\overline{\text{SRES}}$	$\overline{\text{RESET}}$	Out	Reset signal
34	DS0	$\overline{\text{DSO}}$	—	Dot display controller SO
35	$\overline{\text{SHEN}}$	$\overline{\text{SHEN}}$	Out	Shift enable signal
36	$\overline{\text{IRQ}}$	$\overline{\text{KRQ}}$	Out	Key request signal
37	KR0	$\overline{\text{KR0}}$	In	Key return signal
38	KR1	$\overline{\text{KR1}}$	In	Key return signal
39	KR2	$\overline{\text{KR2}}$	In	Key return signal
40	KR3	$\overline{\text{KR3}}$	In	Key return signal
41	RESET	CKDCR	In	CKDC reset signal
42	OSC2	OSC2	—	Clock
43	OSC1	OSC1	—	Clock
44	GND	GND	—	GND
45	CL1	CL1	—	Time clock
46	CL2	CL2	—	Time clock
47	TEST	VCKDC	—	+5V
48	G0	G1	Out	Display digit signal
49	G1	G2	Out	Display digit signal
50	G2	G3	Out	Display digit signal
51	G3	G4	Out	Display digit signal
52	G4	G5	Out	Display digit signal
53	G5	G6	Out	Display digit signal
54	G6	G7	Out	Display digit signal
55	G7	G8	Out	Display digit signal
56	G8	G9	Out	Display digit signal
57	G9	G10	Out	Display digit signal
58	G10	G11	Out	Display digit signal
59	G11	NC	Out	NC
60	PO0	NC		NC
61	PO1	NC		NC
62	PO2	NC	—	NC
63	PO3	NC	—	NC
64	SA	SA	—	Segment A

2-10. ISP2032

This IC has been developed specially for UP-3300 to achieve VGA CHIP and PSRAM interfaces.

Pin description

Pin No.	Name	I/O	Function
1	/VMEM	In	VIDEO MEMORY DECODE C00000H ~ C1FFFFH 16bit/8bit access, 8 bit read from the CPU is treated as 16-bit on the VGA.
2	/VMEM2	In	VIDEO MEMORY DECODE (ONLY FOR GRAPHICS MODE; 8BIT) C80000H ~ C9FFFFH 8-bit access only. /VMEM and /VMEM2 differ in their apparent address to each other, but the contents of memory to be accessed are the same. They differ in access method (WORD/BYTE).
3	/HWR	In	HIGH BYTE WRITE FROM CPU
4	/LWR	In	LOW BYTE WRITE FROM CPU
5	PHAI	In	CLOCK FROM CPU
6	VCC		
7	/ISPEN	In	for ISP (In System Program)
8	/VWAITI	In	WAIT FROM VGA CHIP (IOCHRDY)
9	/VWAIT	Out	WAIT TO MPCA There are following 2 ORs. ① IOCHRDY from VGA CHIP ② 1 WAIT is generated when VRAM. VGA I/O is accessed. (Because IOCHRDY is slow, 1 WAIT is generated prior to it.)
10	/DWRI	In	DELAYED WRITE (FOR VGA CHIP TIMING)
11	/DWRO	Out	WRITE FOR /DWRI
12	/DRDI	In	DELAYED READ (FOR VGA CHIP TIMING)
13	/DRD	Out	READ FOR /PRDI
14	RES	Out	RESET OUTPUT RESET ← NOT (/RESET)
15	/RES	In	/RESET INPUT
16	A0	In	A0
17	GND		
18	A20	In	A20
19	PCE21E	Out	EXTENDED PSRAM1 DECODE (EVEN) 800000H ~ 8FFFFFFH
20	PCE21O	Out	EXTENDED PSRAM1 DECODE (ODD) 800000H ~ 8FFFFFFH
21	PCE22O	Out	EXTENDED PSRAM2 DECODE (ODD) 900000H ~ 9FFFFFFH
22	PCE22E	Out	EXTENDED PSRAM2 DECODE (EVEN) 900000H ~ 9FFFFFFH
23	/IPLON0	In	IPL SIGNAL
24	/PSRF0	Out	PSRAM REFRESH
25	/OWR	Out	PSRAM WRITE (ODD SIDE)
26	/M3SWP	Out	MODE3 BUS SWAP (FOR PSRAM ACCESS WHEN IPL)
27	Y2/SCLK		ISP
28	VCC		
29	Y1/RESET		ISP
30	MODE		ISP

Pin No.	Name	I/O	Function
31	RASPN2E	In	EXTENDED PSRAM2 DECODE (FROM MPCA) 800000H ~ 9FFFFFFH
32	RASPN2	In	EXTENDED PSRAM2 DECODE (FROM MPCA) 800000H ~ 9FFFFFFH
33	/RASPN12	In	PSRAM DECODE (FROM MPCA) 600000H ~ 9FFFFFFH
34	/AS	In	/AS FROM CPU
35	/RD	In	/RD FROM CPU
36	/RFSH	In	/RFSH FROM CPU
37	/SMEMR	Out	VIDEO MEMORY READ (TO VGA CHIP)
38	/SMEMW	Out	VIDEO MEMORY WRITE (TO VGA CHIP)
39	GND		
40	/COE0		Not used
41	/IORD	Out	VGA IO READ (TO VGA CHIP)
42	/IOWR	Out	VGA IO WRITE (TO VGA CHIP)
43	/SBHE	Out	BUS HIGH ENABLE (TO VGA CHIP)
44	/VIO2	Out	VGA IO CHIP SELECT

3. Address map

3-1. Total memory space

The address map of the total memory space is shown below. As you can see, the memory space is divided into the following 5 blocks:

- 0page area (including the I/O area)
- VRAM
- RAM
- ROM
- Extended I/O area

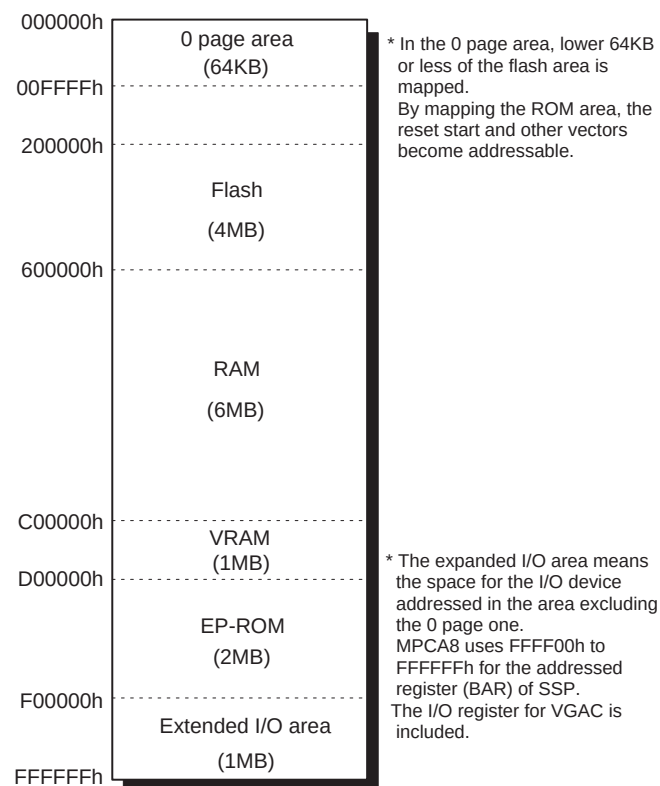


Fig. 2

3-2. 0page area

The 0page area consists of four spaces: the ROM mapped area, internal and external I/O areas.

The ROM mapped space have been devised for the following purposes:

- ① Simplifying the procedure for booting the IPL program
- ② Achieving high-speed accessing, and accessing by abbreviated instructions.

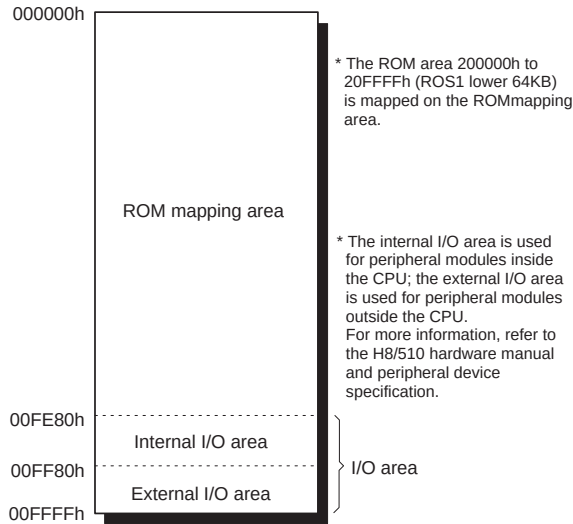


Fig. 3

3-3. I/O areas

The addresses from 00FF80h to 00FFFFh are called the internal I/O area.

The internal I/O area is a space where the control registers and built-in ports inside the CPU are addressed.

The external I/O area is a space where the peripheral devices outside the CPU or devices on an optional card are addressed.

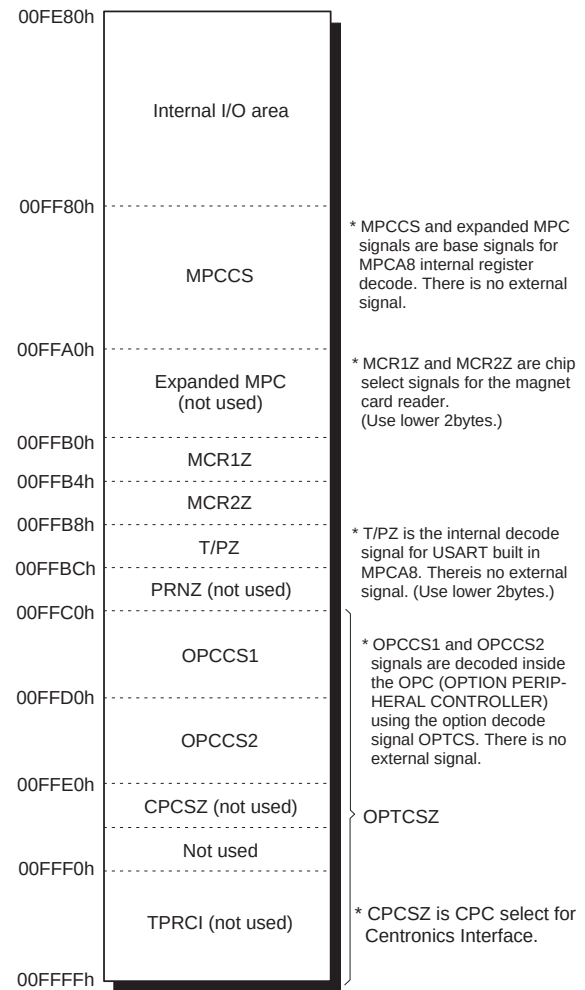


Fig. 4

3-4. ROM space

Fig.5 shows the ROM space. The UP-3300 uses 2MB of NOR-type flash memory instead of conventional ROM, so that the ROS1 from the MPCA8 is input into the chip enable of the flash memory.

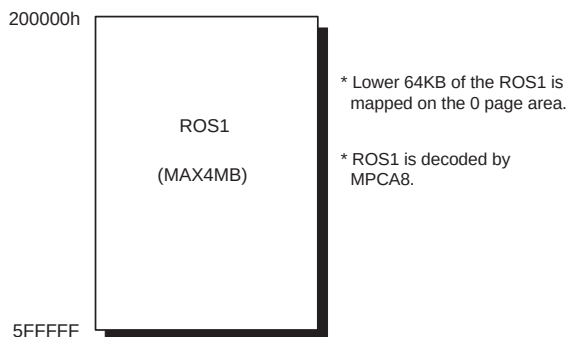


Fig. 5

3-5. VRAM & RAM space

The VRAM is the display memory of the LCD.

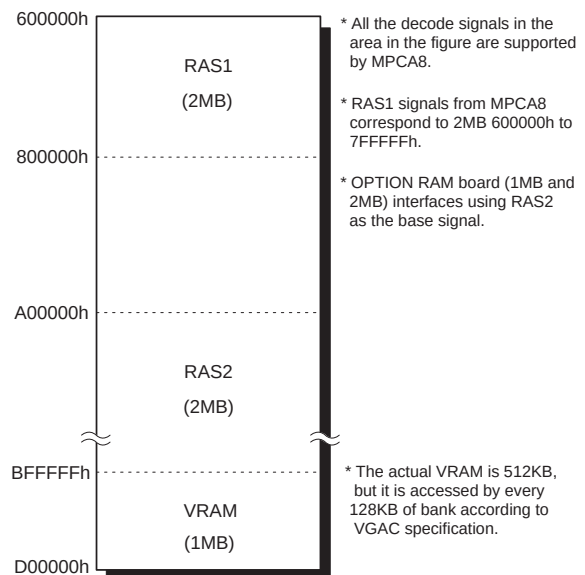


Fig. 6

3-6. Extended I/O area

The addresses from F00000h to FFFFFFFh are called an extended I/O area. The UP-3300 uses the following addresses as the break address register (BAR) for SSP.

- FFFF00h ~ FFFFFFFh

4. LCD display

The main display is a 640 × 480 dot liquid crystal display.

4-1. Block diagram

Here is the block diagram of the LCD and its allied components.

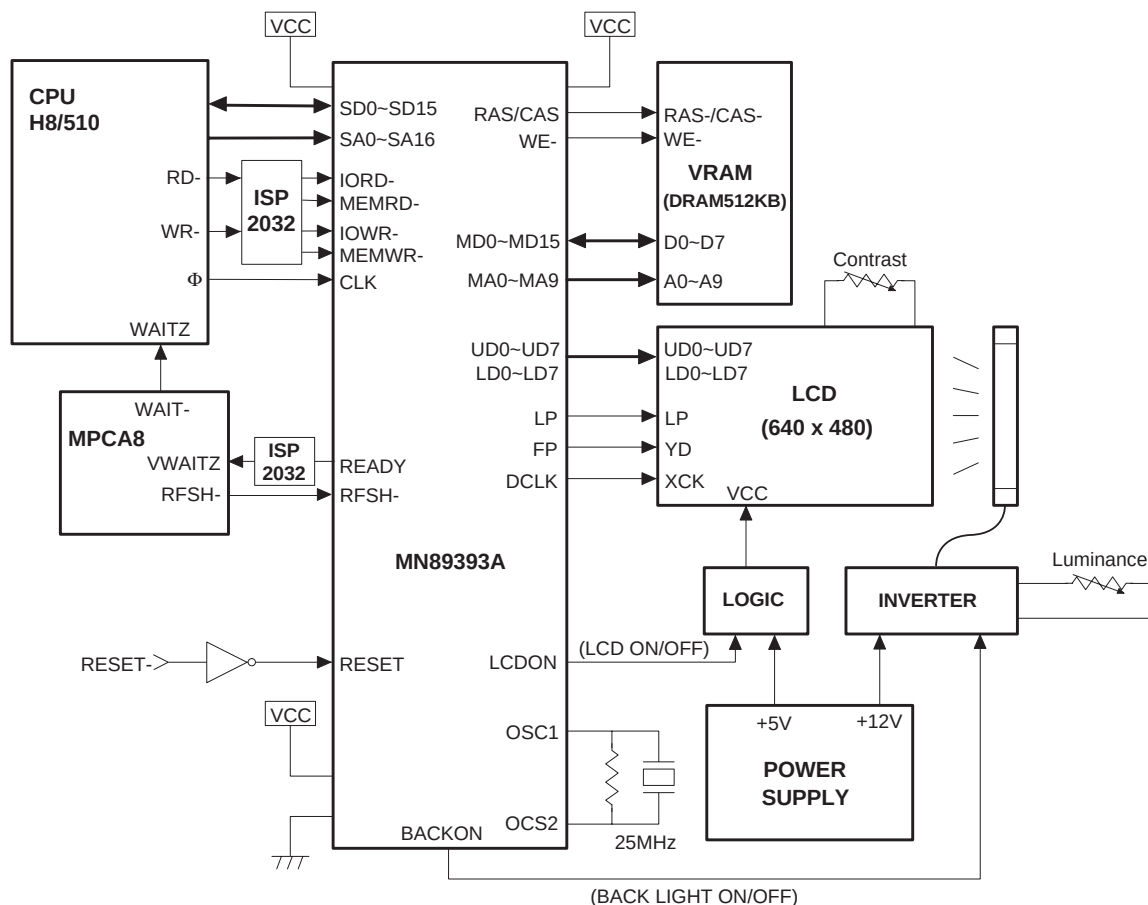


Fig. 7

4-2. LCD panel

The dot-matrix LCD unit LM10V33 with color STN and CCFT back light is used for LCD panel. It provides 640 × 480 resolution.

4-3. Display controller

Matsushita VGAC (MN89303A) is used for display controller.

VRAM is on the address space of the CPU and data can be written on and read from it by every 128 KB of bank at the address C00000H ~ C1FFFFH from the CPU side. VRAM consists of 4 banks.

4-4. LCD ON control

The LCD's bias power supply is controlled by the MN89303A terminal LCDON to turn the LCD screen on and off.

The LCDON is at "L" at resetting +5V power is supplied to the LCD by setting the expanded function control register bit5 of MN89303A to "H" with software. The LCD screen isn't turned on until +5V is supplied.

4-5. Back light control

The back light is turned ON/OFF by the MN89303A terminal BACKON. The initial value is "L" and the back light is off. By setting the expanded function control register bit6 of MN89303A to "H", the inverter unit is turned on.

4-6. Luminance and contrast adjustment

- Luminance: Luminance is adjusted with an inverter which has dimming function.
- Contrast: Contrast is adjusted by controlling the contrast adjustment voltage (VCON) of the LM10V33.

5. Customer display

The customer display uses the NEW TYPE 2 LINE vacuum fluorescent tube. The display is turned on and off by the CKDC9.

6. Pseudo SRAM (Standard)

The device is TOSHIBA 4MB SRAM (TC51V8512AFT 512K × 8bit) with access time of 120ns.

6-1. CPU interface

The figure below shows a typical pseudo SRAM interface in the up-3300.

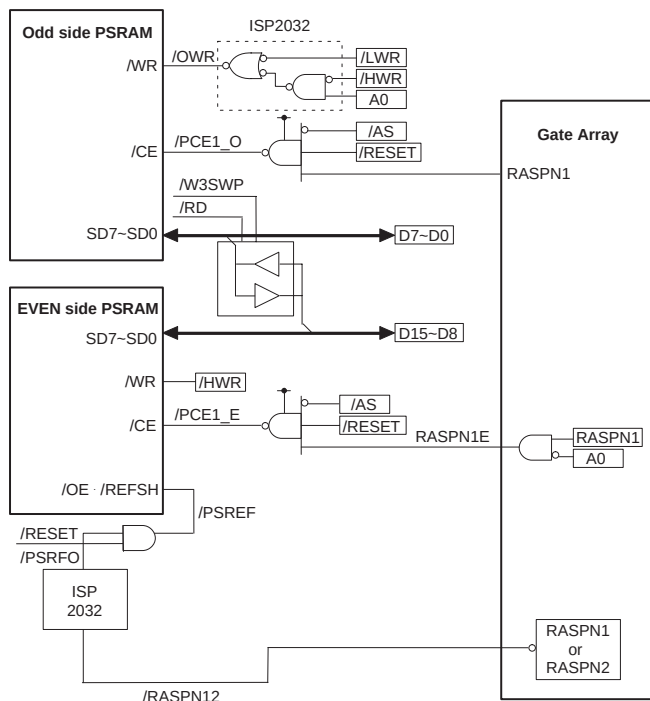


Fig. 8

6-2. Pseudo SRAM address

Standard pseudo SRAM is decoded as follows by the RASPN1 signal.

- ① 700000h ~ 7FFFFFFh

The base signal is 2MB. It thus wraparounds with 600000H ~ 6FFFFFFH 1MB.

Pseudo SRAM consists of 1 chip for respective even and odd number addresses. Both of word and byte access from CPU are available.

7. NOR-type flash memory

Here is the explanation for the interface of NOR-type flash memory. The device is Sharp's LH28F016SU flash memory which consists of 512 K words × 16 or 1 MB × 8, with 16 blocks of 64 KB.

7-1. CPU interface

The figure below shows a typical interface for the LH28F016SU of the up-3300 system.

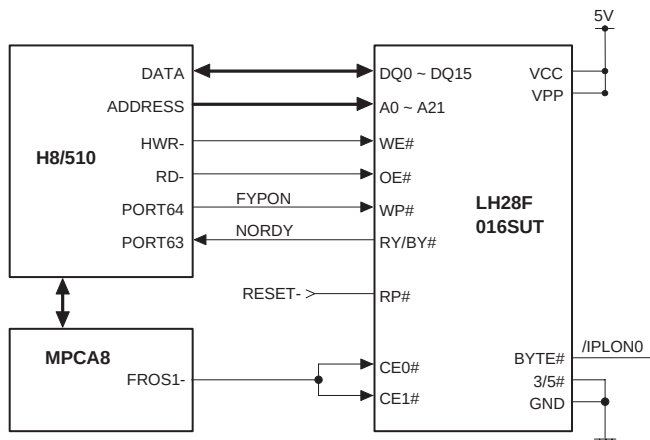


Fig. 9

7-2. Device control

After resetting, the device automatically enters the array read mode and perform the same action as the usual ROM, thus requiring no special consideration when reading data.

Data can be written at high speed by using the page buffer.

8. SSP control

The UP-3300 uses flash memory in the place of EPROM, so it is possible to rewrite the contents of the flash memory in changing the program. However, since the existing gate array MPCA8 is used, it is also possible to use the conventional SSP.

8-1. Operation

Like the MPCA7, the MPCA8 adopts the break address register comparison method for detecting addresses. The operation of this method is briefly explained below.

The gate array always compares the break address register (BAR) built in the gate array, with the address bus to monitor the address bus.

If both agree, the gate array outputs the NMI signal to the CPU, which in turn shifts from normal handling to exception handling.

In both the MPCA7 and the MPCA8, SSP is achieved by the above operation.

The setting of the break address register (BAR) is directly written in the addresses from FFFF00h to FFFFFFFh.

9. Interrupt control

There are roughly two types of interrupts:

- Internal interrupts: Controlled inside the CPU
- External interrupts: Input into the CPU from outside

9-1. Internal interrupts

Device interrupts built in the CPU are used for the following applications:

Table 8

Event factor	Application
SC11	Interrupt source as IR channel
SC12	Not used (SC1 is used for CKDC interface.)
FRT1 (ICI) (OCRA) (OCRB) (OVF)	INTMCR ~ MCR interrupt (to FT11 terminal)
FRT2 (ICI) (OCRA) (OCRB) (OVF)	Standard SHEN event (for CKDC) Simple IRC timer event RS232 timer event System timer (53 ms)
TMR (CMA) (CMB) (OVF)	
WDT (OVF)	Drawer open timer
A/D	Not used
NMI	SSP request

9-2. External interrupts

The following types of external interrupts are available:

- NMI (SSP)
- IRQ0 (Standard I/O interrupt)
- IRQ1 (RS232 interrupt)
- IRQ2 (Used as SCK terminal)
- IRQ3 (Used as SCK terminal)

10. WAIT control

The weight control function built in the MPCA8 is used to provide an interface with low-speed devices.

10-1. Block diagram

The block diagram of the wait control function is shown.

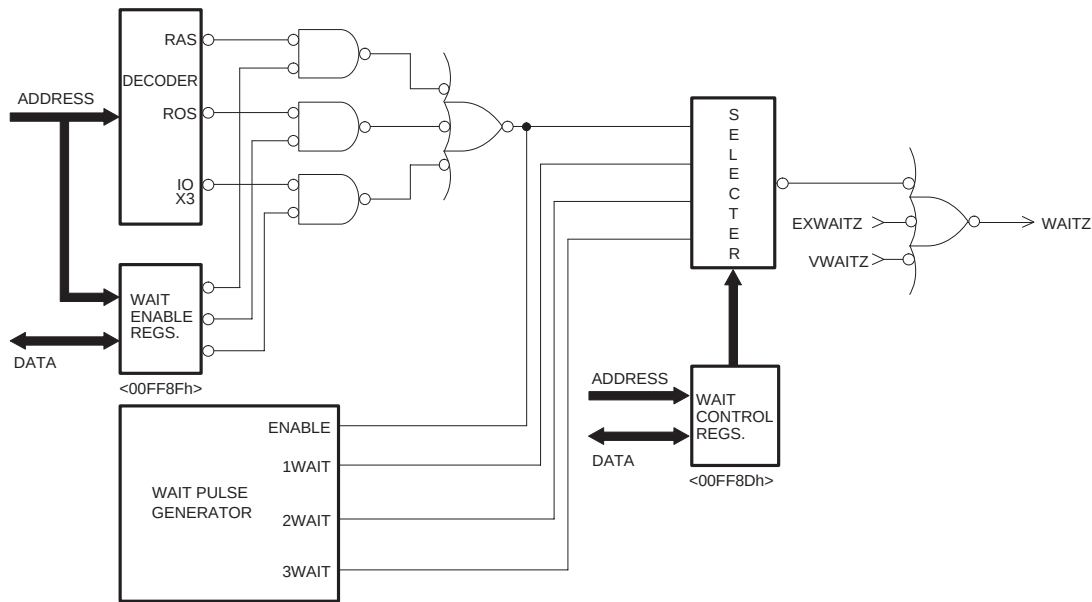


Fig. 10

In the figure, the decoder, wait enabling register, AND-OR sections are the same as those in the MPCA6 or 7, but other components are newly incorporated in the MPCA7.

EXWAITZ and WAITZ are external weight signals which are to be Ored inside the MPCA8 and output to the WAITZ. The EXWAITZ is a general-purpose wait request terminal, and WAITZ is the wait request signal from the VGA controller.

11. CKDC9

The UP-3300 performs the following controls, using CKDC9.

- Customer display
- Clock
- Buzzer
- System reset

11-1 Interface

CKDC9 is connected through the MPCA8.

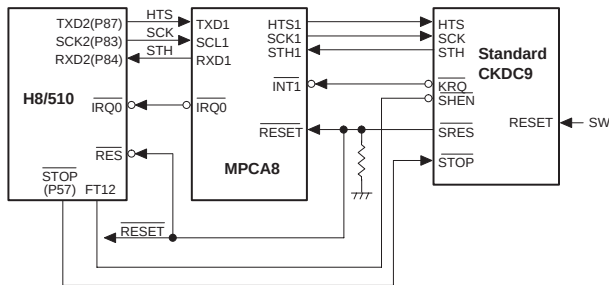


Fig. 11

12. Option RAM interface

12-1. Interface

The expanded RAM connector terminals are shown in the table.

The 72 pin S.O. DIMM is used for the connector.

Extension RAM connector terminals

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
GND	1	—	25	D9	49
GND	2	—	26	D8	50
—	3	—	27	D7	51
—	4	—	28	D6	52
—	5	A13	29	D5	53
—	6	A12	30	D4	54
—	7	A11	31	D3	55
—	8	A10	32	D2	56
—	9	A9	33	D1	57
—	10	A8	34	D0	58
A14	11	A7	35	GND	59
A15	12	A6	36	NC	60
A16	13	A5	37	OWR	61
A17	14	A4	38	—	62
A18	15	A3	39	—	63
A19	16	A2	40	—	64
—	17	A1	41	—	65
PCE22_E	18	A0	42	—	66
PCE21_E	19	D15	43	HWR	67
—	20	D14	44	—	68
PSREF	21	D13	45	VMEM	69
PCE22_O	22	D12	46	VMEM	70
PCE21_O	23	D11	47	GND	71
GND	24	D10	48	GND	72

13. Reset sequence

The reset sequence block diagram is shown below. Note that $\overline{\text{RESET}}$ signal (system reset) and CKDCR signal (CKDC reset) are different from each other.

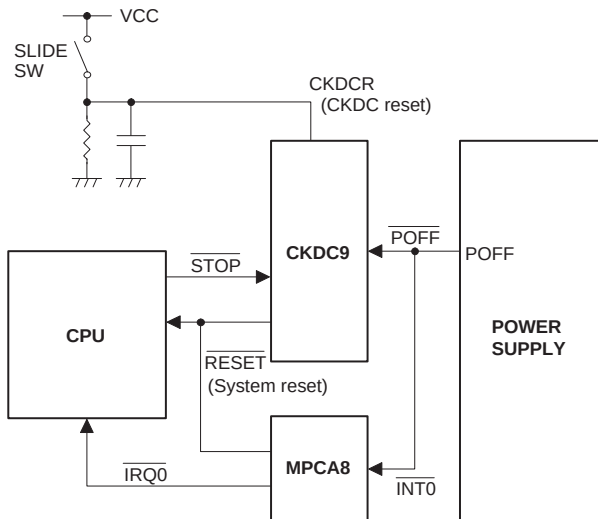


Fig. 14

13-1. Power ON/OFF

The flow of signal processing at the time of the power supply turning On/Off is as follows:

Table 19

<Power OFF>

	Power supply	MPCA8	CPU	CKDC9
1	$\overline{\text{POFF}} \rightarrow \text{L}$			
2		$\overline{\text{IRQ0}} \rightarrow \text{L}$		
3			$\overline{\text{STOP}} \rightarrow \text{L}$	
4				$\overline{\text{RESET}} \rightarrow \text{L}$ (System reset)

Table 20

<Power ON>

	Power supply	MPCA8	CPU	CKDC9
1	$\overline{\text{POFF}} \rightarrow \text{H}$			
2				$\overline{\text{RESET}} \rightarrow \text{H}$ (System reset)

The table below shows the timing chart.

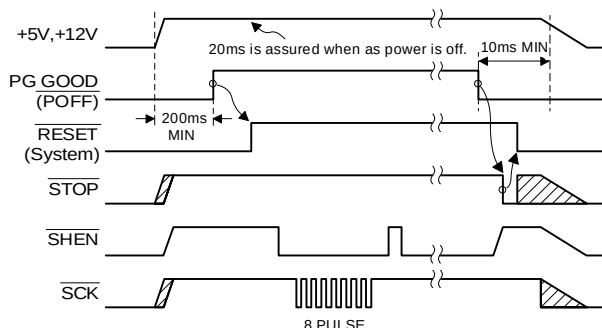


Fig. 15

13-2. MRS, SRV reset

The UP-3300 does not have the mode switch. The procedure for resetting MRS, SRV is different from that of conventional cash registers.

in the UP-3300, MRS, SRV resetting is selected and executed by the key which has been depressed when the CKDC reset is released to start the system.

(In the case of MRS, security is added by a key operation equivalent to a pass word.)

Flow chart

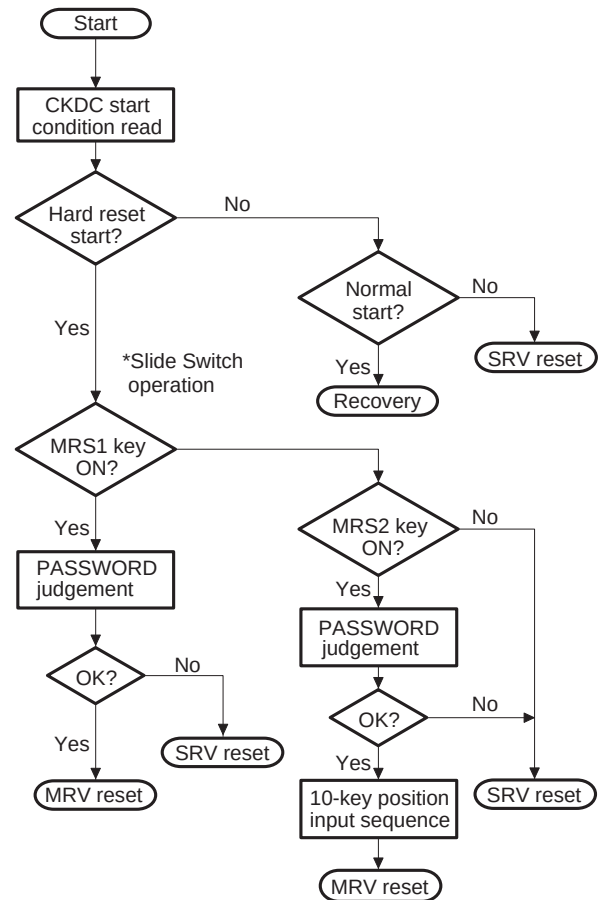


Fig. 16

14. Drawer

The UP-3300 can use up to 2 optional external drawers.

14-1. Drawer solenoid drive

P34 ~ P37 inside the CPU are allocated for the port output of the drawer solenoid drive.

Table 22

Built-in port	Signal name	Remarks
P34	$\overline{\text{DR0}}$	Drawer 1 (optional drawer)
P35	$\overline{\text{DR1}}$	Drawer 2 (optional drawer)
P36	$\overline{\text{DR2}}$	Reserved
P37	$\overline{\text{DR3}}$	Reserved

One port corresponds to one drawer. Theoretically, it is possible to drive multiple drawers at the same time, but this processing must be inhibited softwarewisely because of power supply capacity and driver hardware factors. If a power failure is detected, the drawer solenoid drive must be stopped as soon as possible.

* The drawer solenoid drive time must be controlled in the range of 40 ms to 50 ms by the timer.

14-2. Drawer open/close sense

The drawer open/close sense signal is input into the built-in port of the CPU. the sense signal of an optional drawer sensor is also wired ORed before inputting.

- P33=1: Any of the drawers is open.

15. IR communication

Data is exchanged with the MPCA8 using the channel 1 (SCI1) of the serial communication interface of the CPU.

15-1 CPU interface and modulator/demodulator

Here is its block diagram.

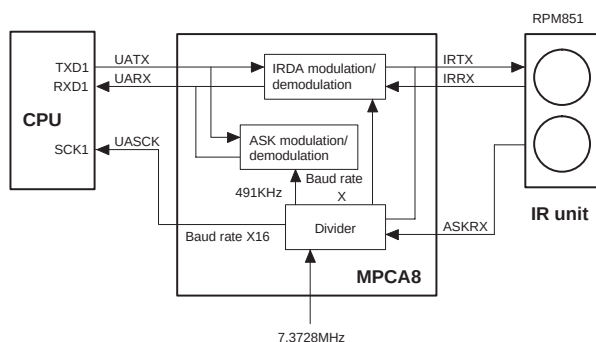


Fig. 20

16. SRN

The SRN of the UP-3300 is compatible with the ER-A750.

17. RS232

Two standard RS232 channels are compatible with the ER-A5RS. However, while the ER-A5RS uses the $\overline{\text{IRQ2}}$ terminal of the CPU for interruption of the RS232, the UP-3300 cannot use the $\overline{\text{IRQ1}}$ terminal instead of it. (The $\overline{\text{IRQ2}}$ terminal is used for IR as the SCK1 terminal.) The standard RS232 is fixed to the logic channels 1 and 2. To the built-in printer, logic channel 7 is assigned. Use the channels 3, 4, 5 and 6 for the ER-A7RS.

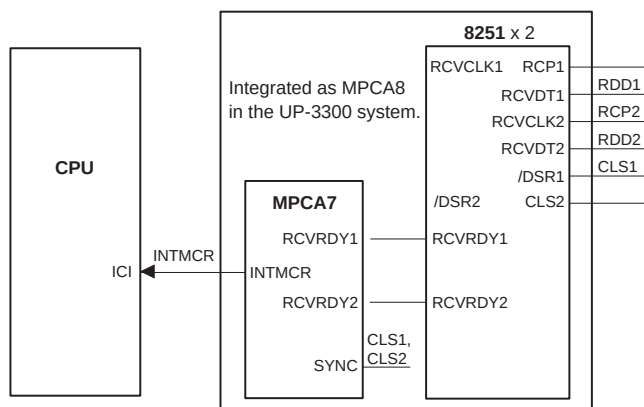
18. MCR

This paragraph describes MCR option (UP-E12MR2) control defined by UP-3300 hardware architecture.

2 channels of the serial port (interchangeable with 8251) built in the MPCA8 are used. 2 tracks of data are read simultaneously. Supports the first and second tracks MCR of ISO. (UP-E12MR2)

18-1. CPU interface

The CPU interface for the USART (8251) and magnet card reader (MCM-21) in the UP-3300 system is shown below.



Signal description

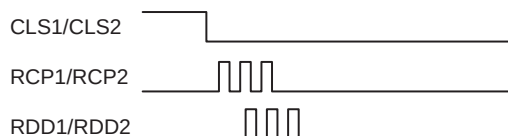
RCP1	TRACK 1 CLOCK PULSE
RDD1	TRACK 1 DATA SIGNAL
RCP2	TRACK 2 CLOCK PULSE
RDD2	TRACK 2 DATA SIGNAL
CLS1	TRACK 1 CARD DETECTION SIGNAL
CLS2	TRACK 2 CARD DETECTION SIGNAL
RCVRDY1	TRACK 1 DATA RECEIVING SIGNAL
RCVRDY2	TRACK 2 DATA RECEIVING SIGNAL
INTMCR	INTERRUPT SIGNAL OR-SYNTHESIZED from RCVRDY and SYNC input

2 chip select signals for 8251 are generated inside MPCA8. The 8251 write recovery time is as follows:

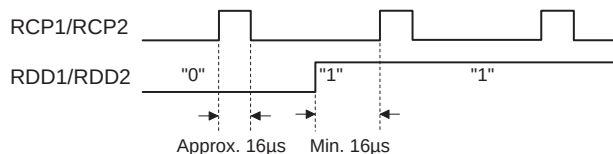
18-2. MCR interface

The operating timing of the MCR interface signals is given below.

(1) Example of timing



(2) Detailed timing (relation between DATA and CLOCK PULSE)



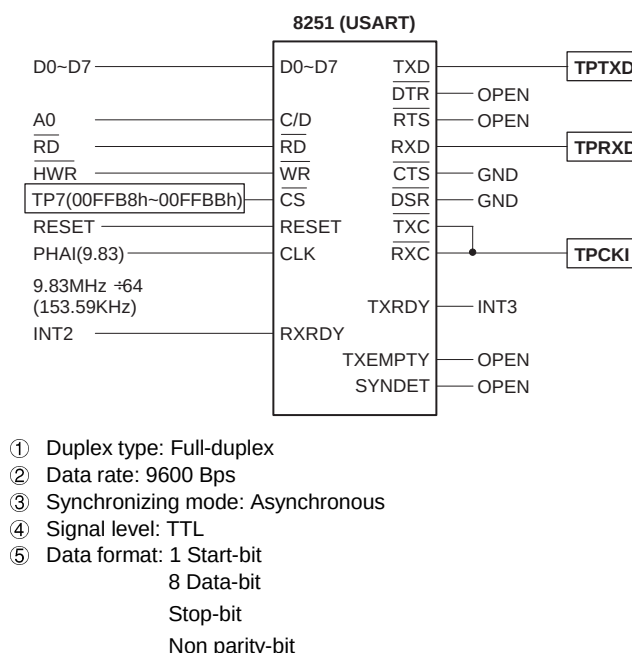
The "NULL" CODE is basically written prior to the opening code. The opening code detection algorithm is considered because data may become corrupt before and after the CARD detection signal due to a worn magnet stripe.

19. Touch panel interface

The 8251 built in the MPCA8 is used as serial communication with the touch panel controller.

8251 (TPZ): Located in 00FFB8h ~ 00FFBBh.

Interrupt: Signal sending interrupt is connected to the INT3.
Signal receiving interrupt is connected to the INT2.

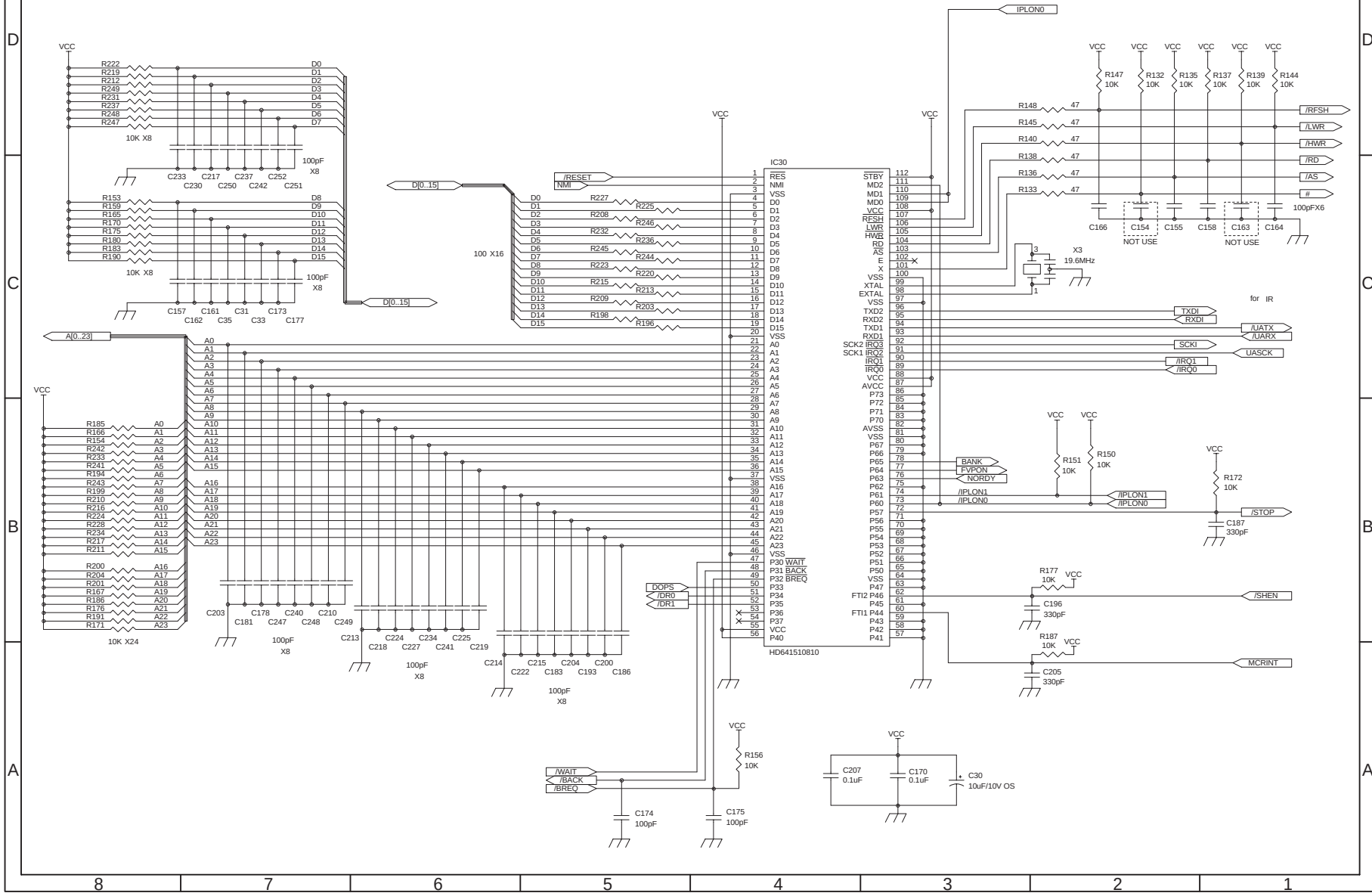


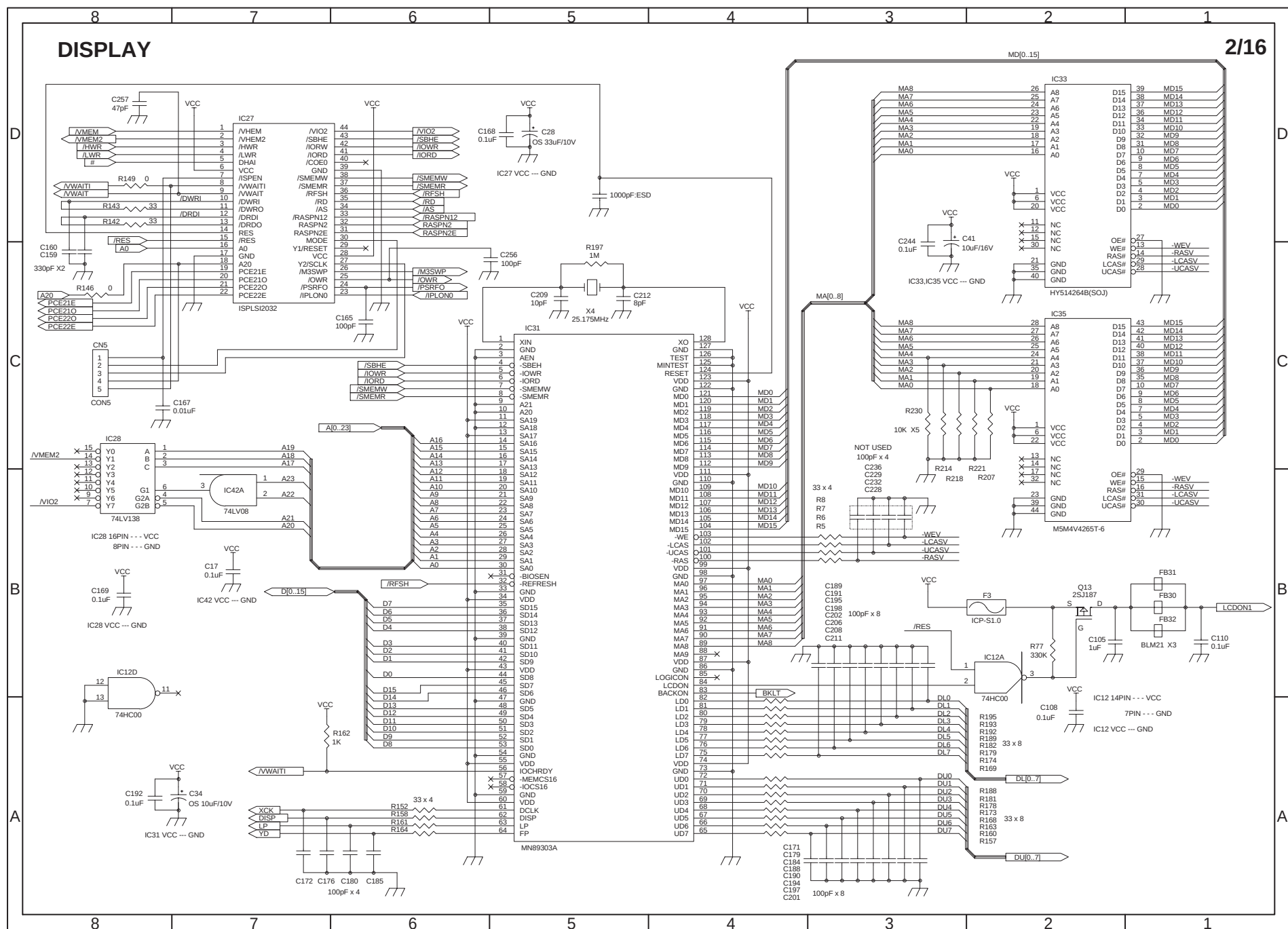
- ① Duplex type: Full-duplex
- ② Data rate: 9600 Bps
- ③ Synchronizing mode: Asynchronous
- ④ Signal level: TTL
- ⑤ Data format: 1 Start-bit
8 Data-bit
Stop-bit
Non parity-bit

CHAPTER8. CIRCUIT DIAGRAM

1. Main PWB

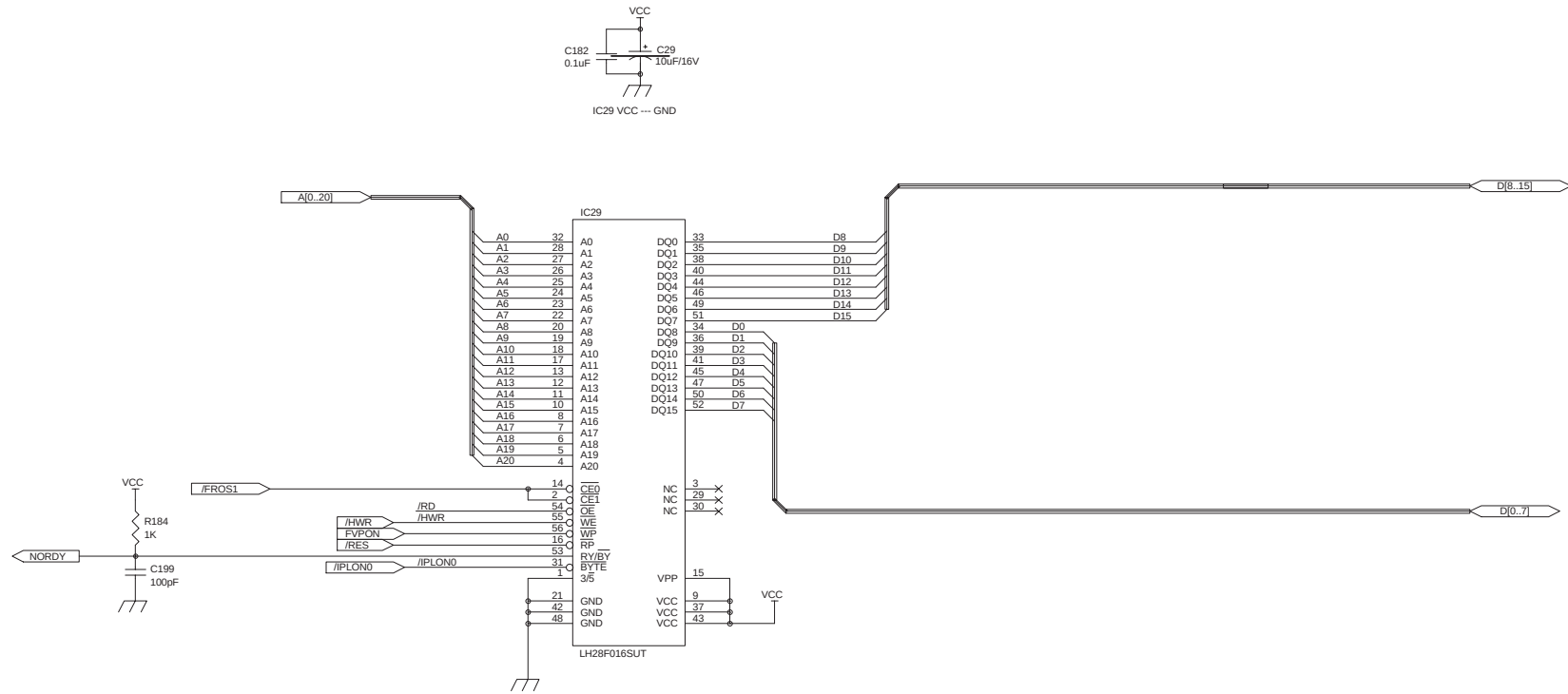
1/16





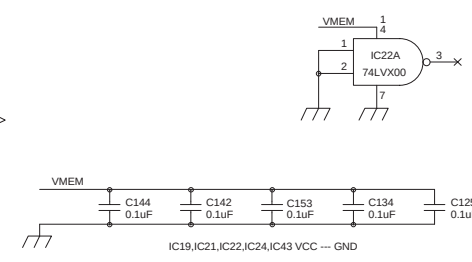
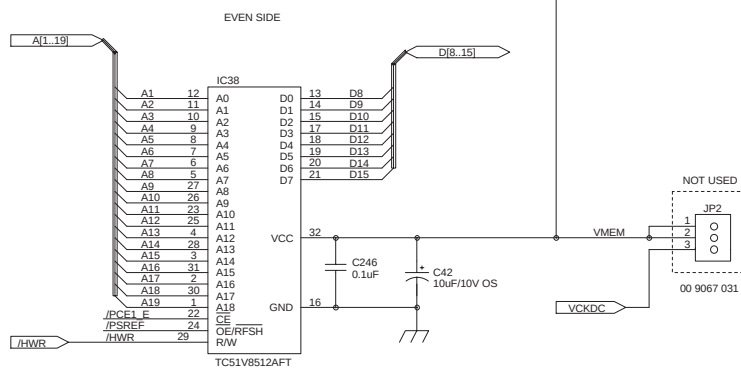
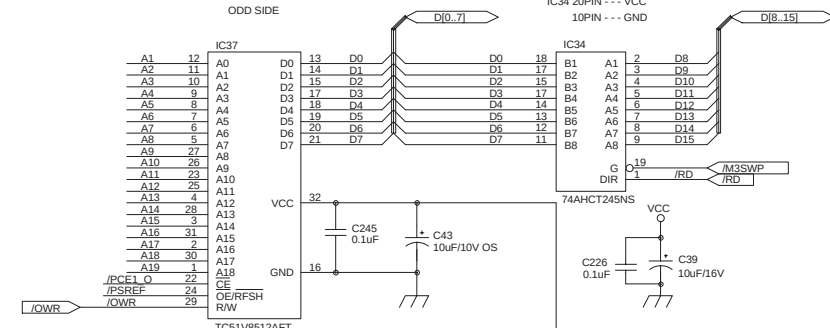
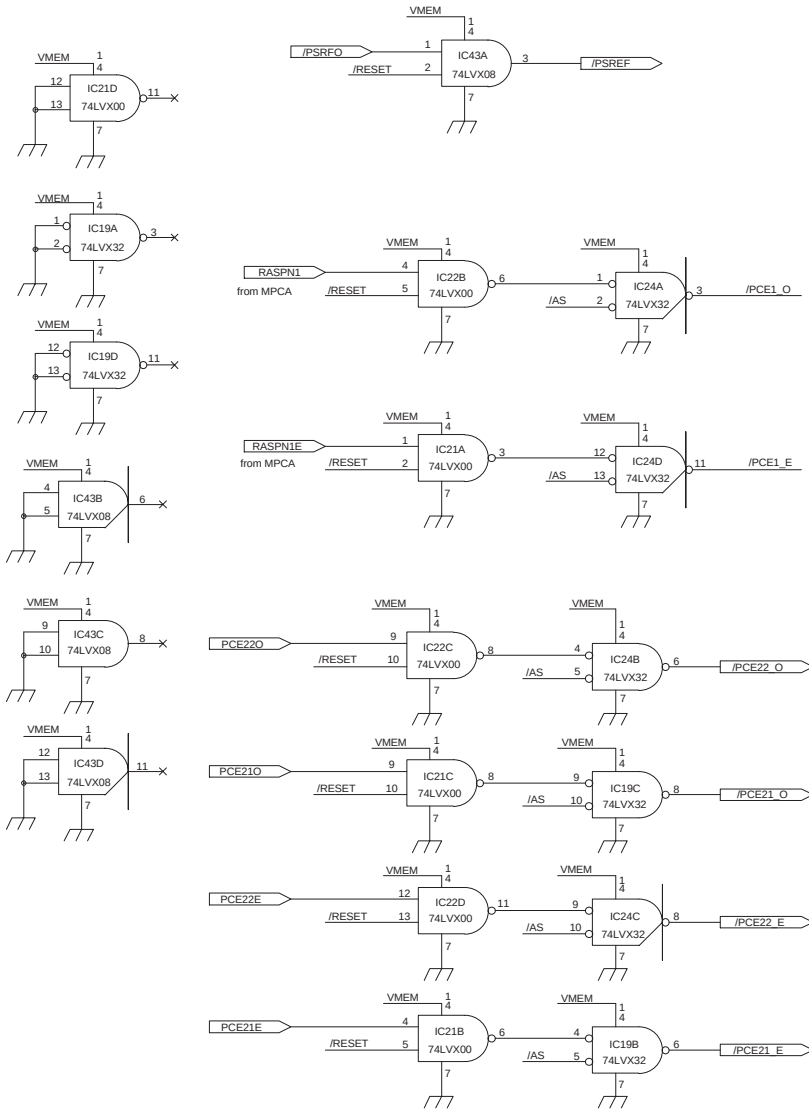
FLASH ROM

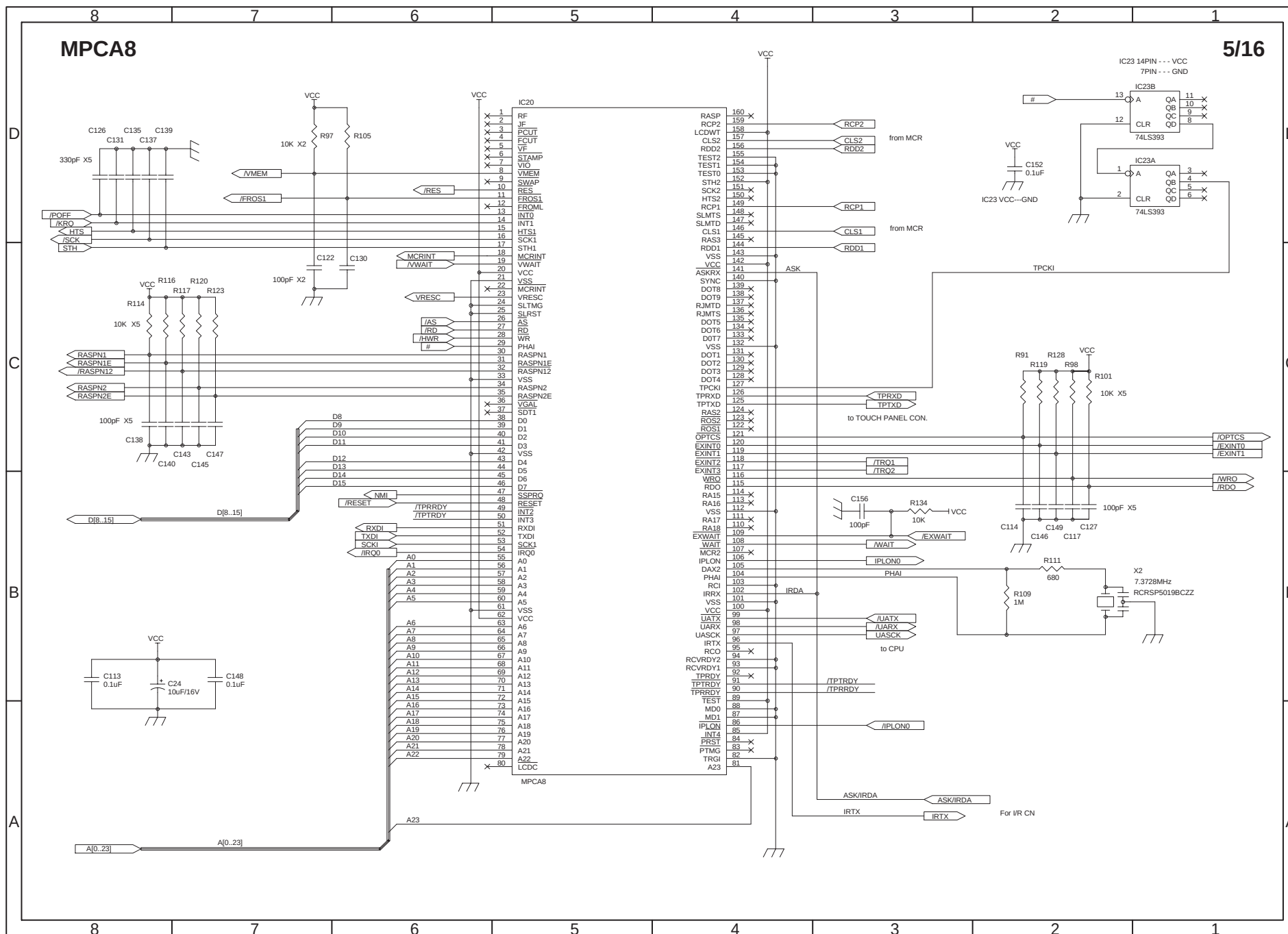
3/16



PSRAM

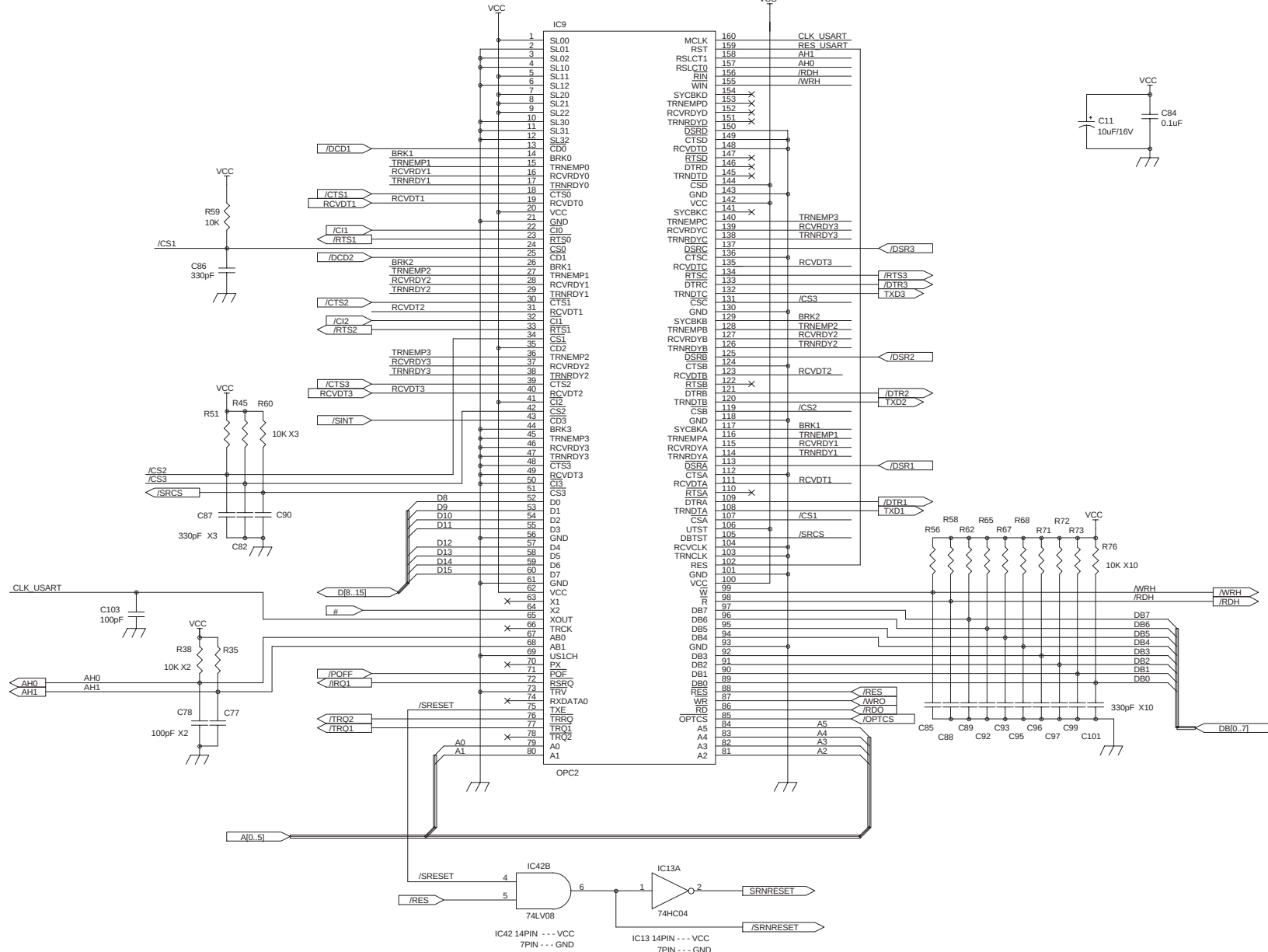
4/16





OPC2

6/16

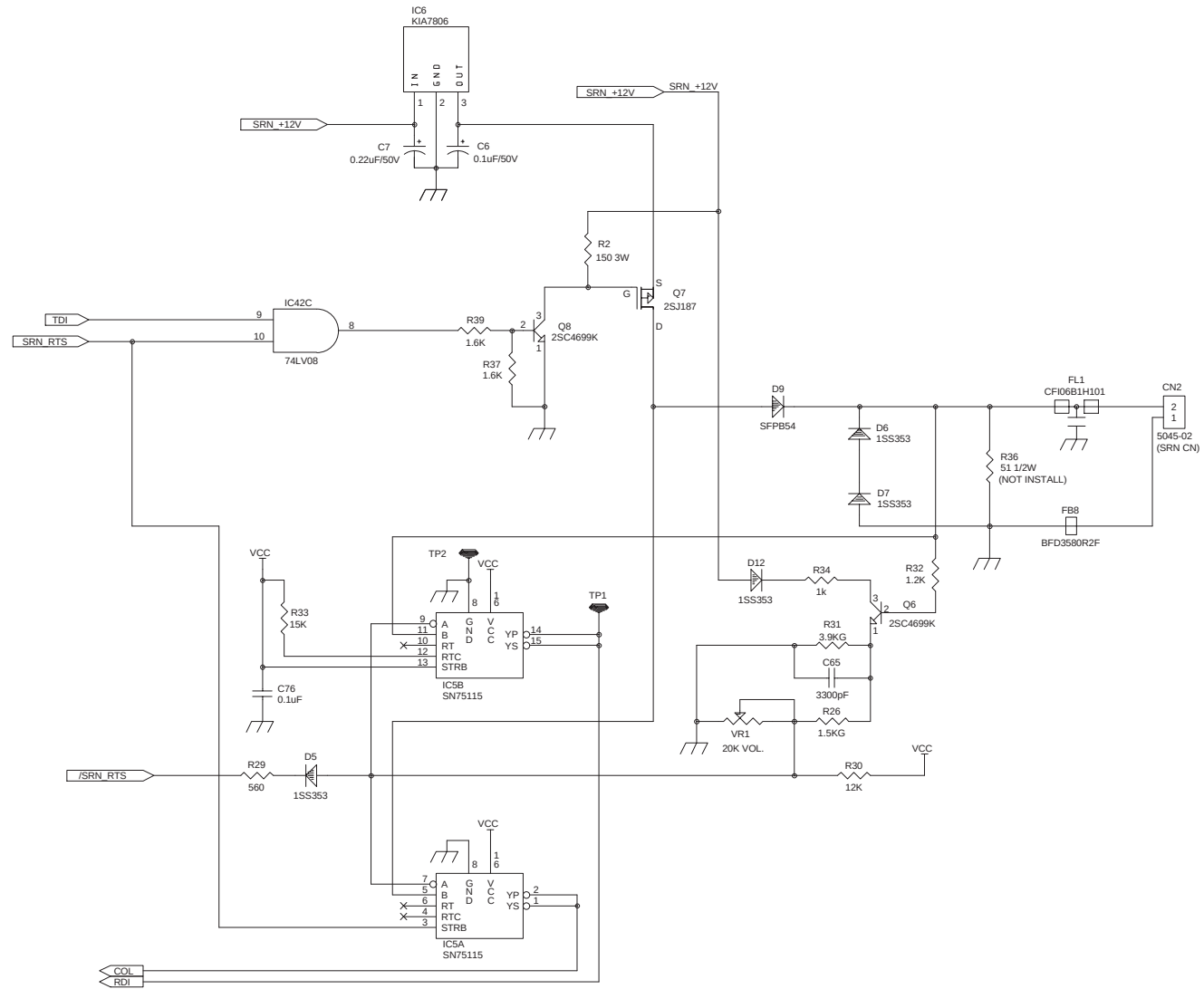
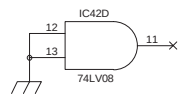






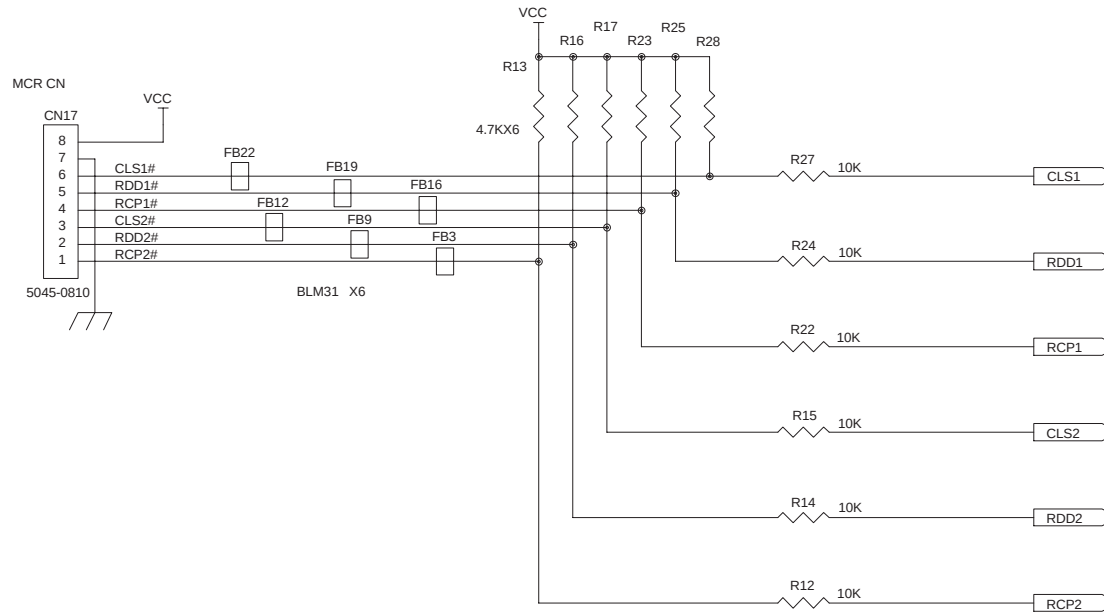
SRN2

9/16



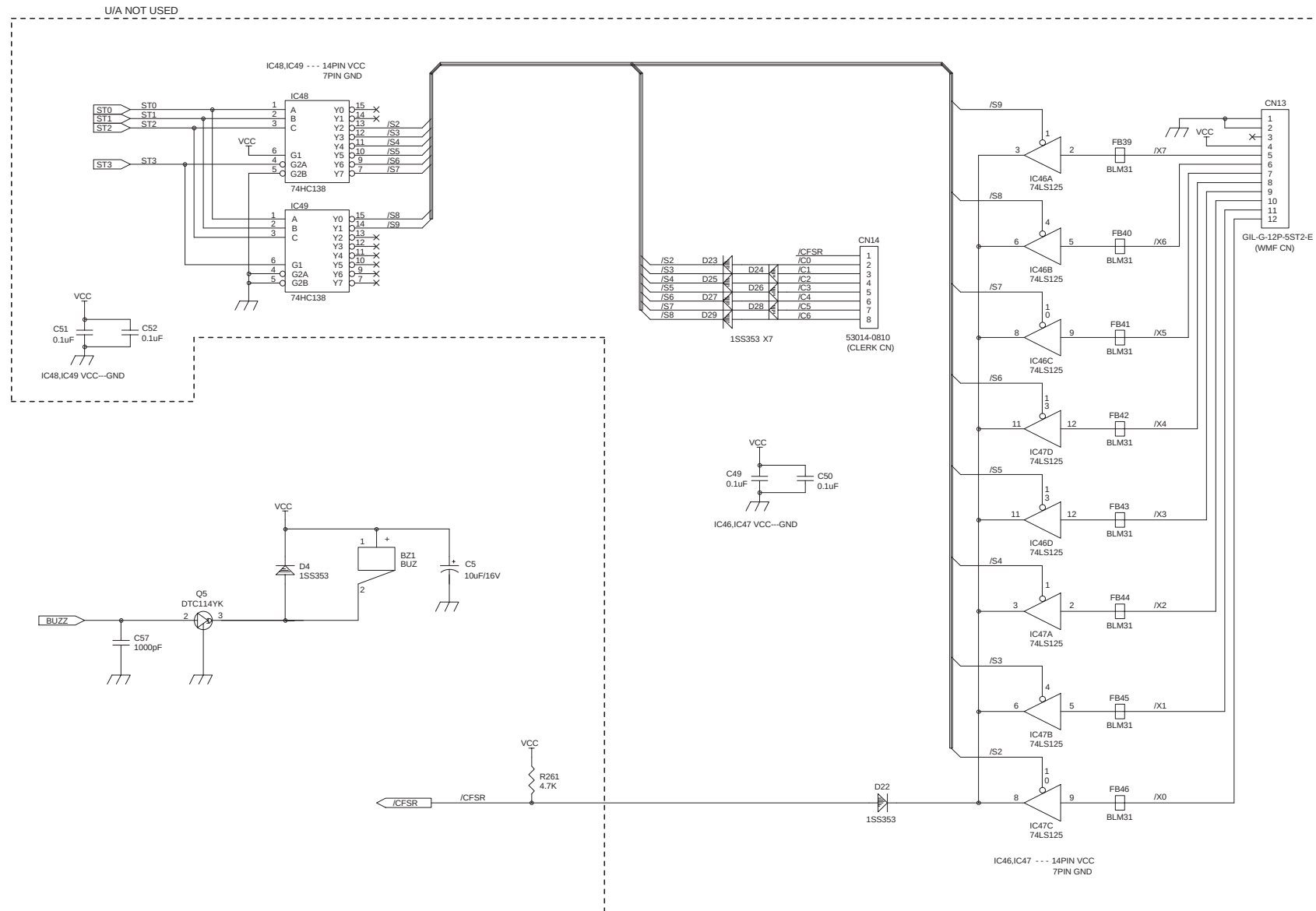
MCR I/F

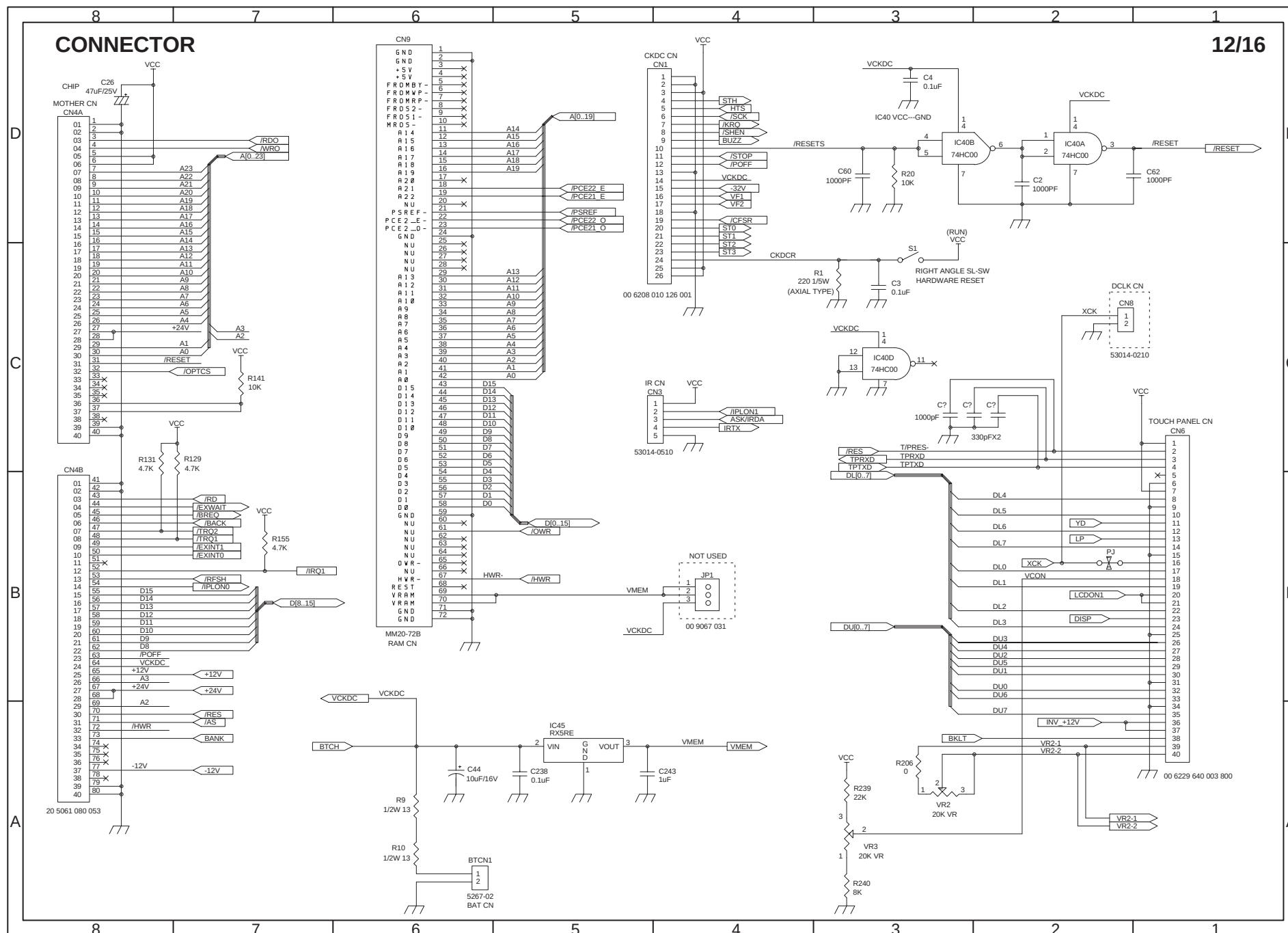
10/16



CLERK I/F

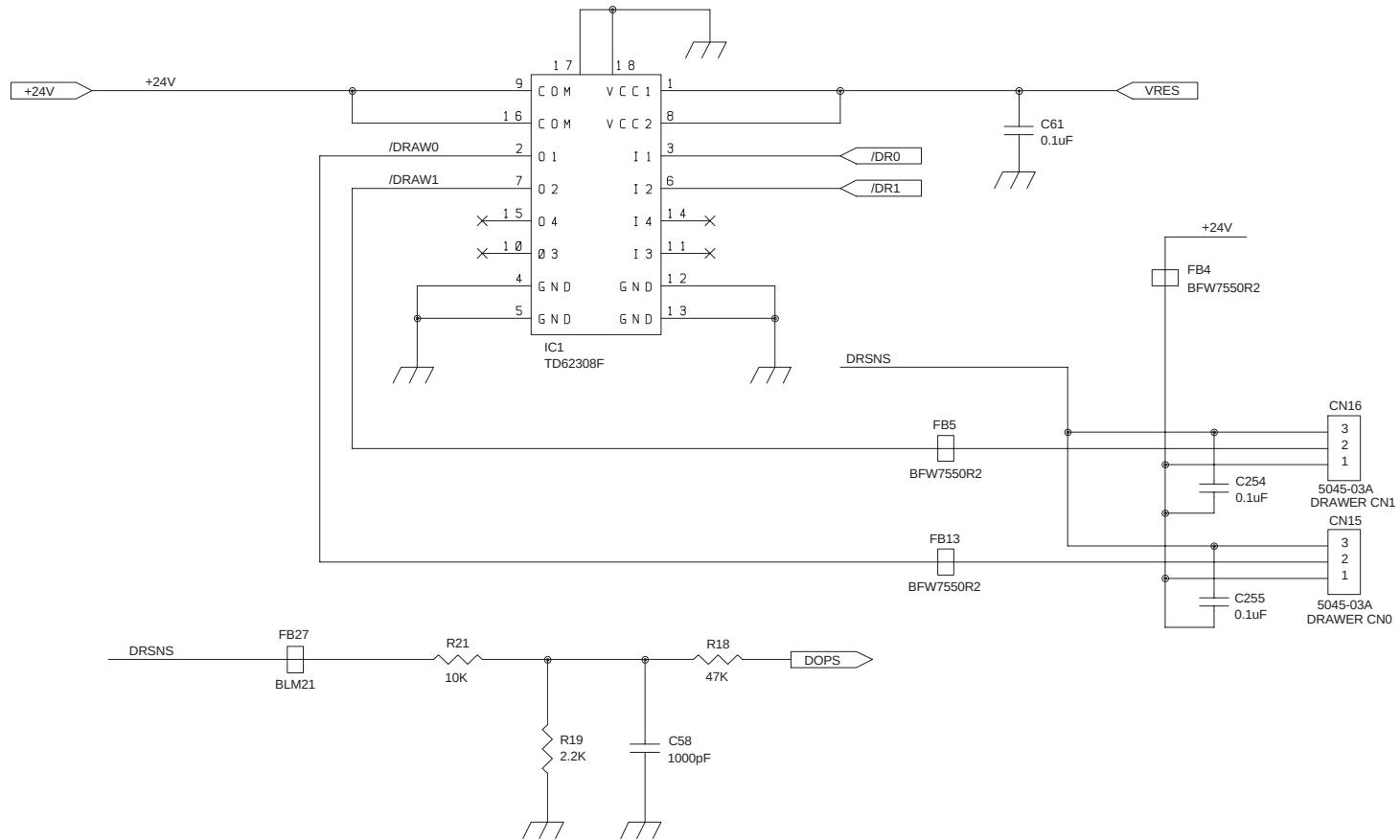
11/16





DRAWER

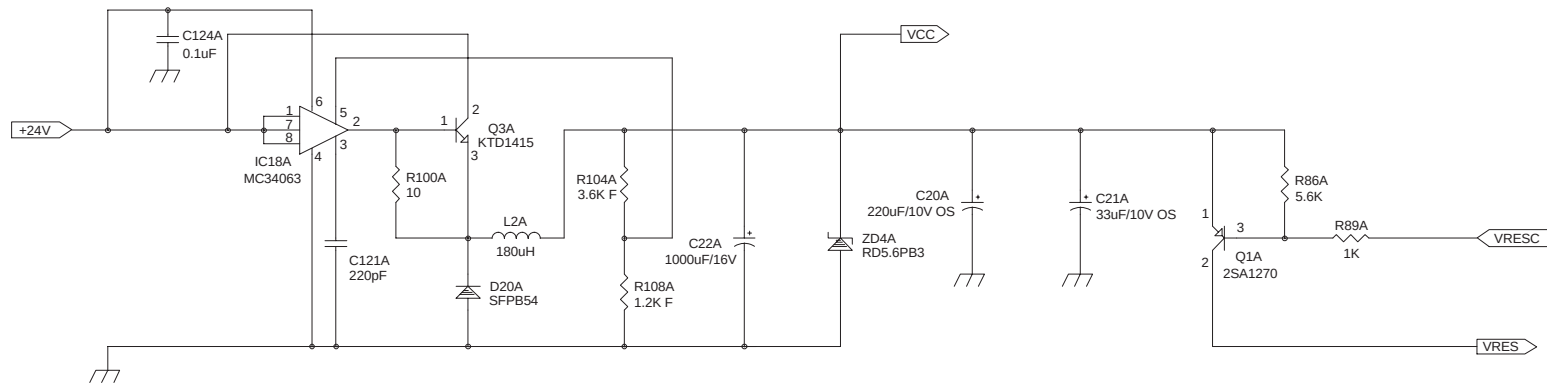
13/16



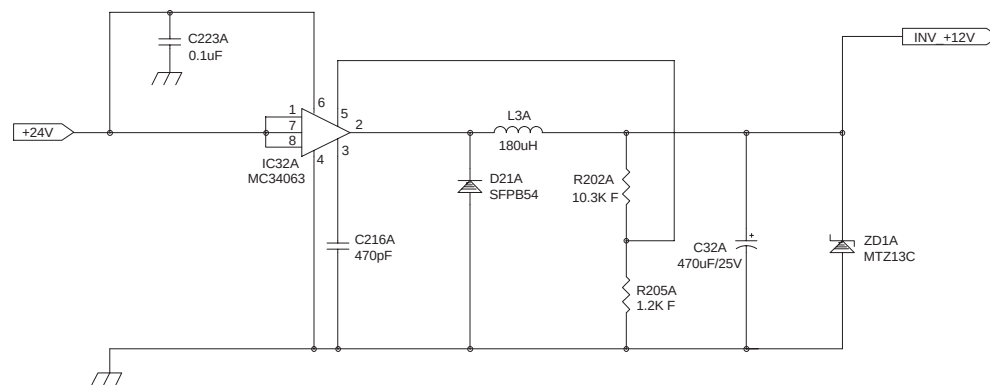
VCC/INV_+12V CIRCUIT

14/16

[VCC POWER CIRCUIT]

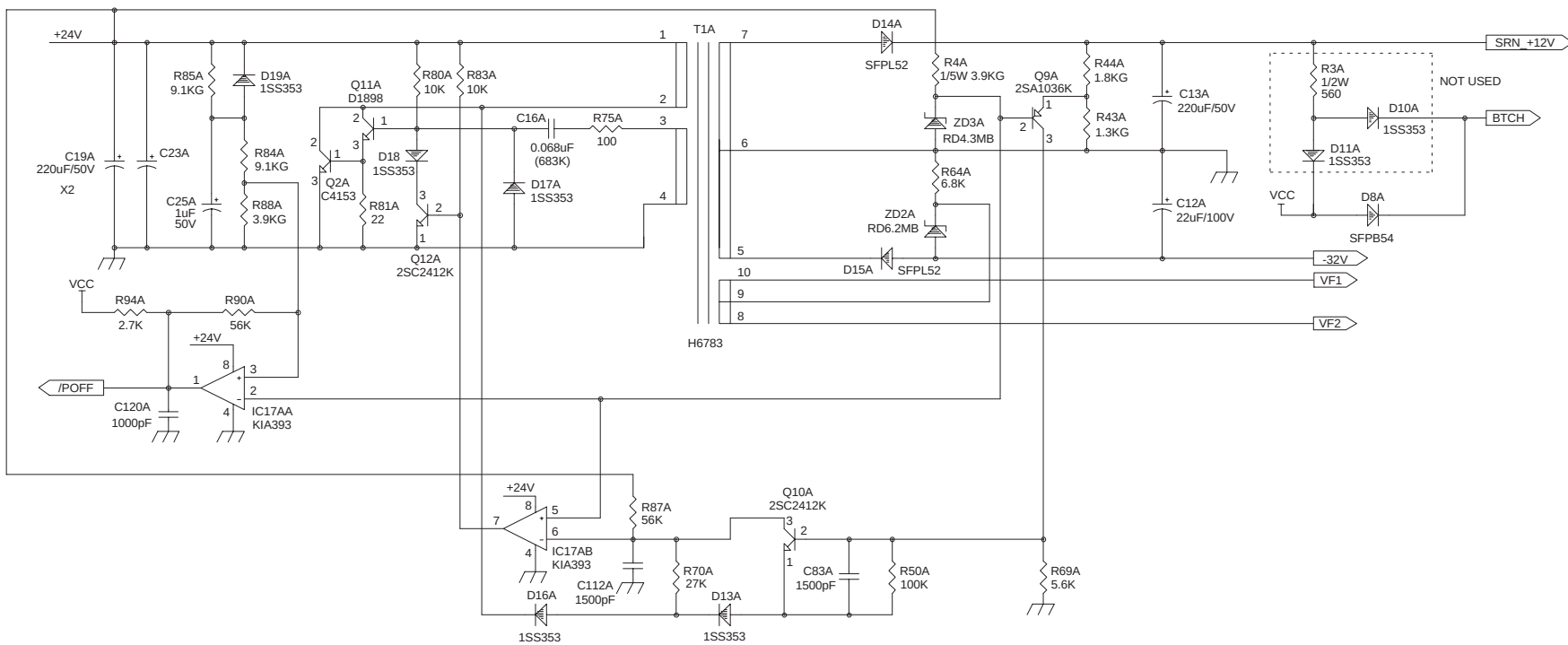
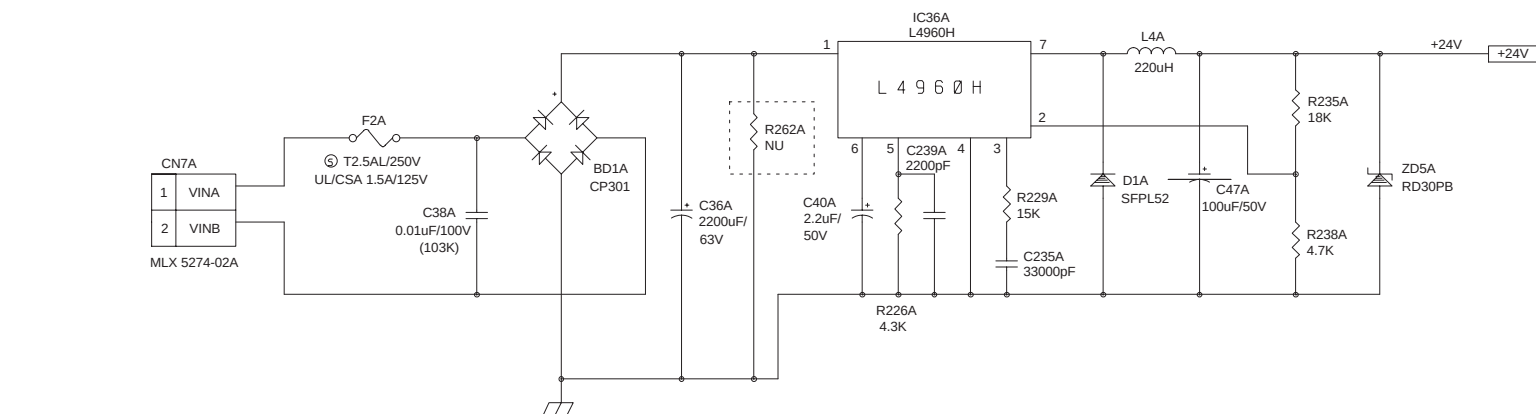


[INV_+12V POWER CIRCUIT]



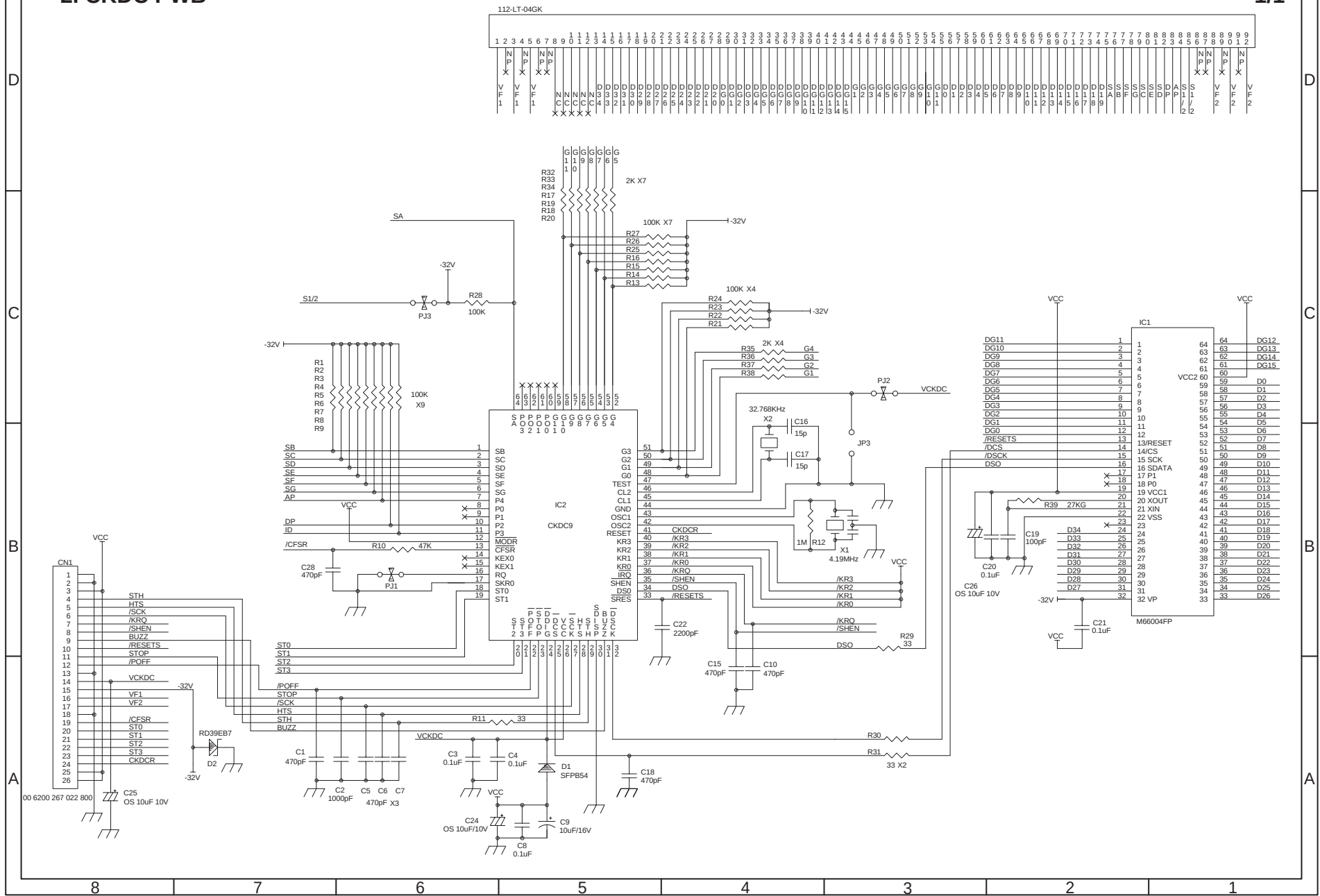
+24V POWER CIRCUIT

16/16



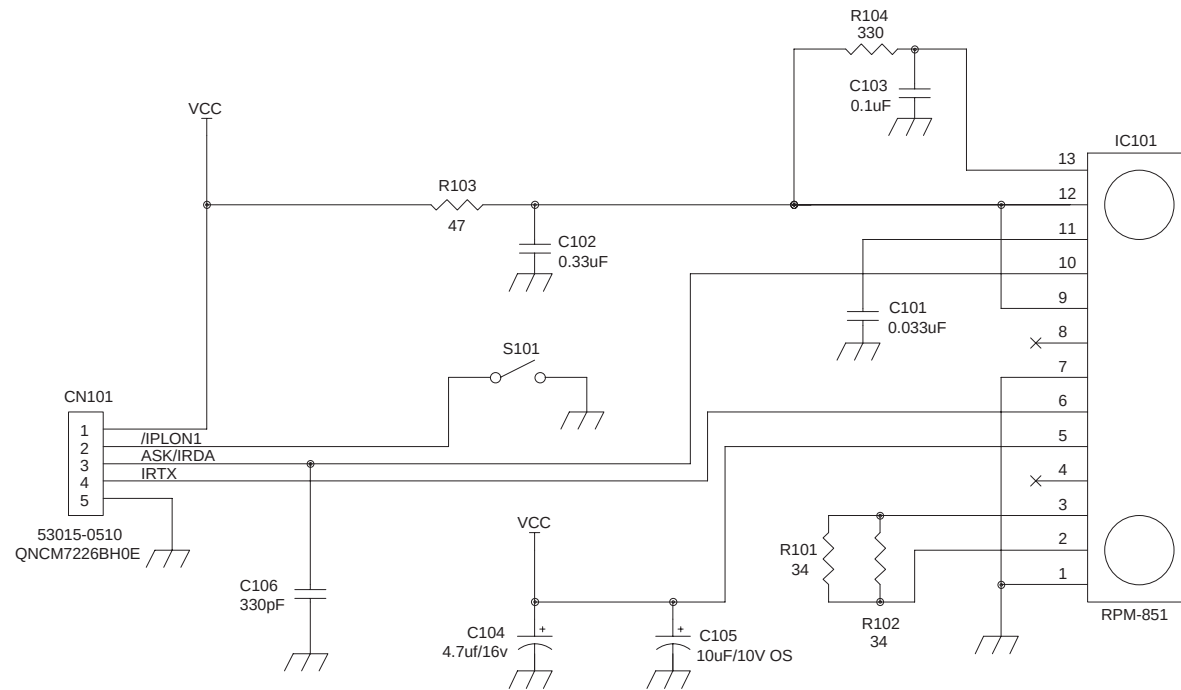
2. CKDC PWB

1/1



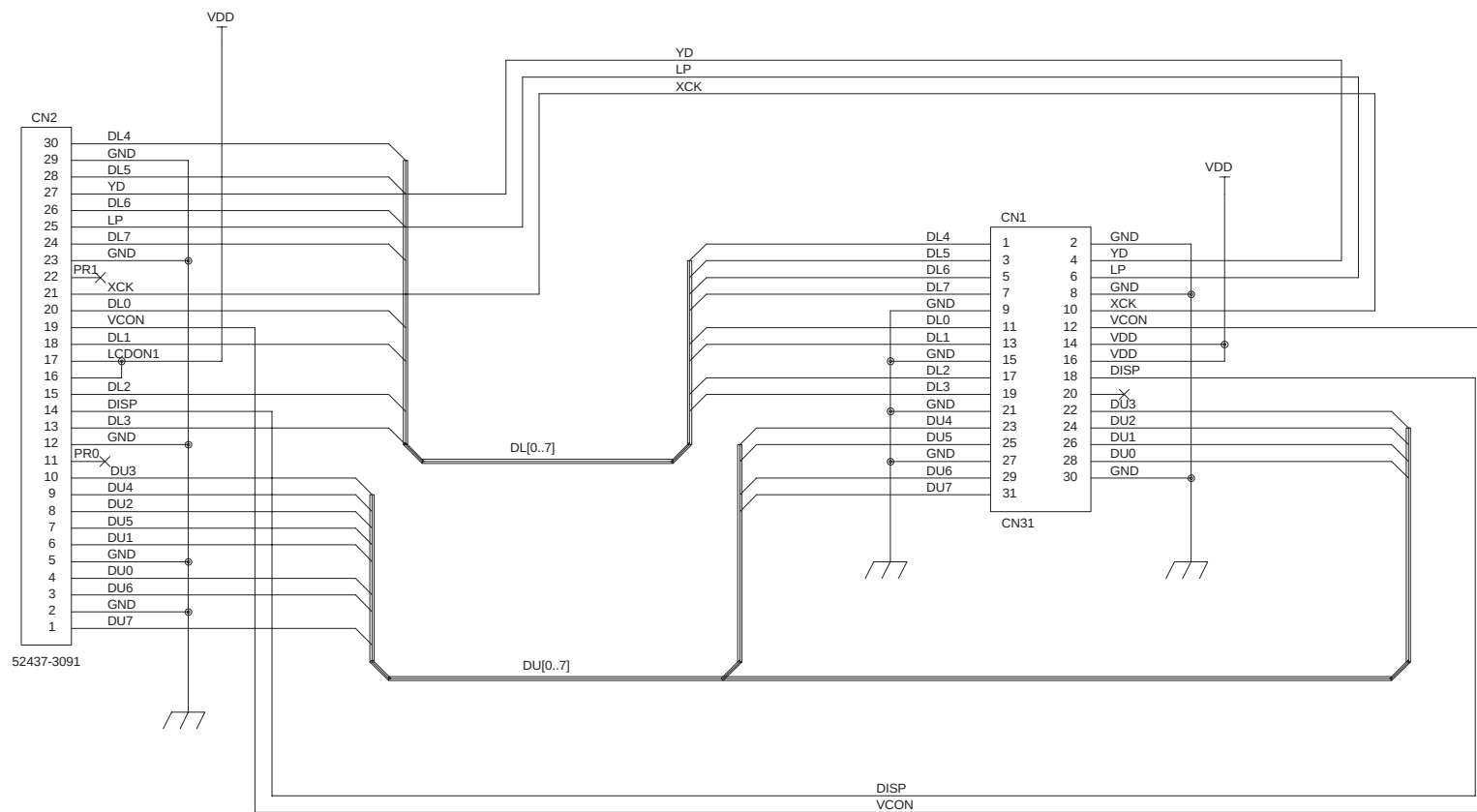
3. IR PWB

1/1



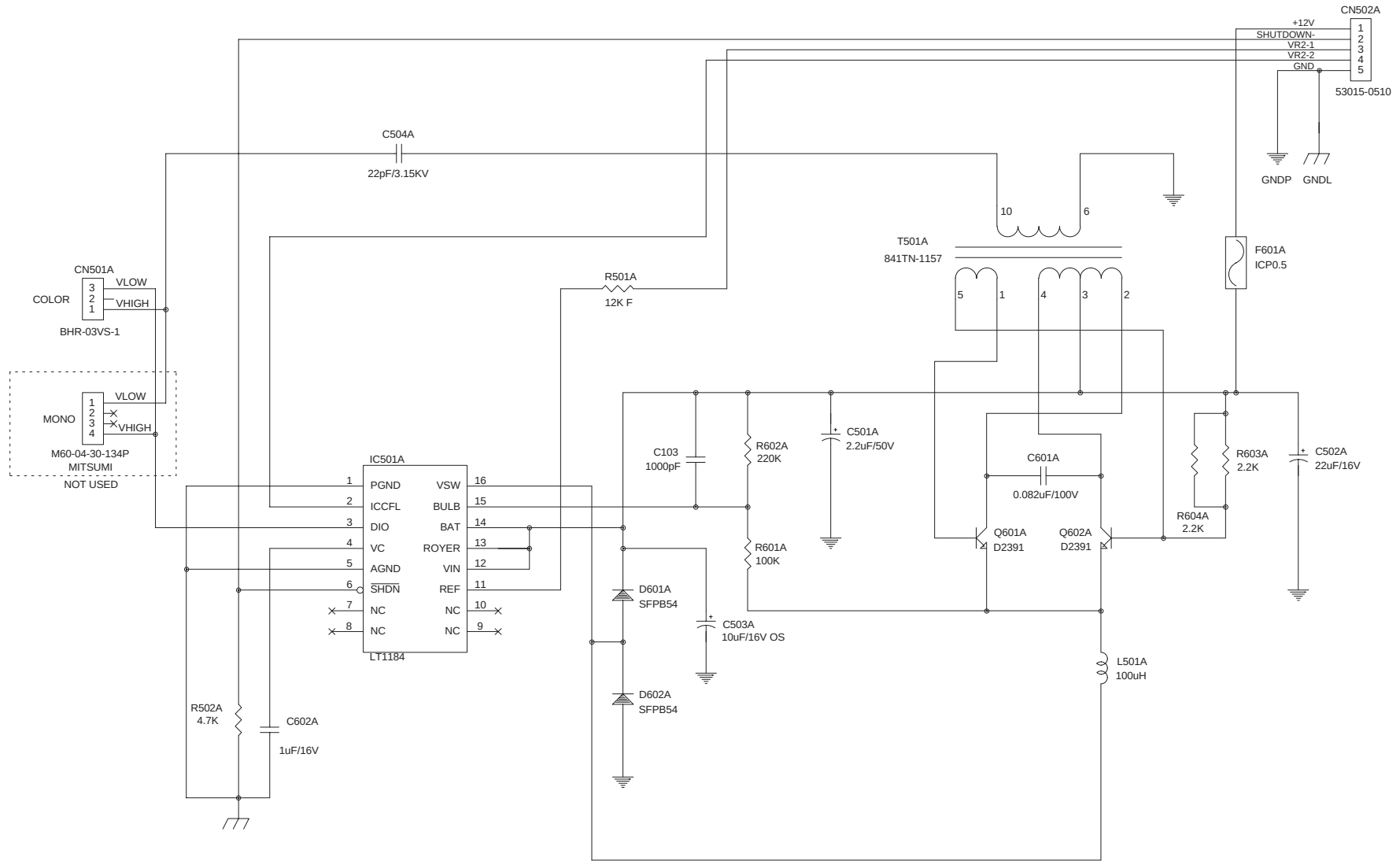
4. LCD PWB

1/1



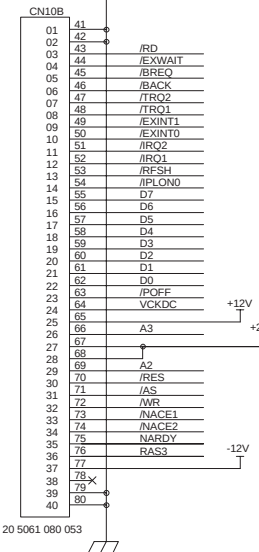
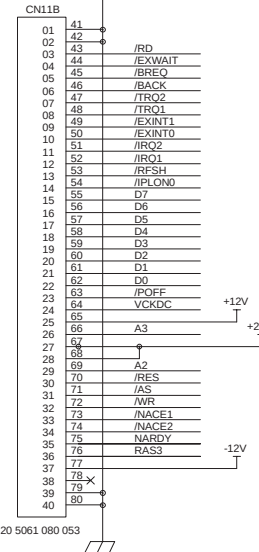
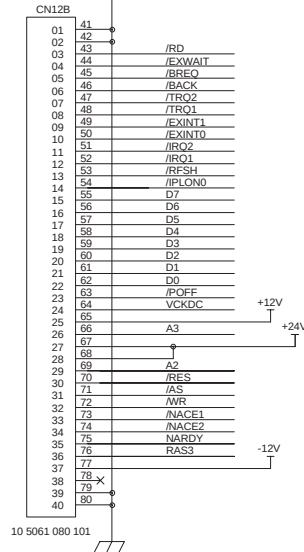
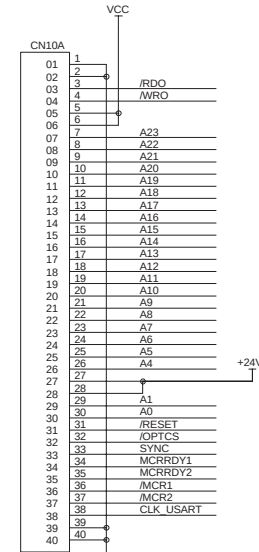
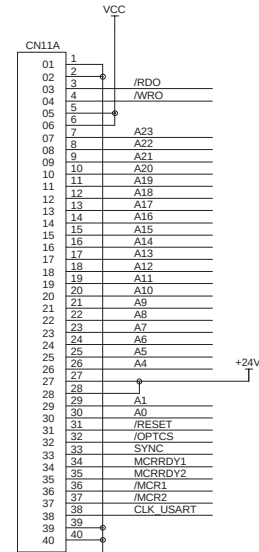
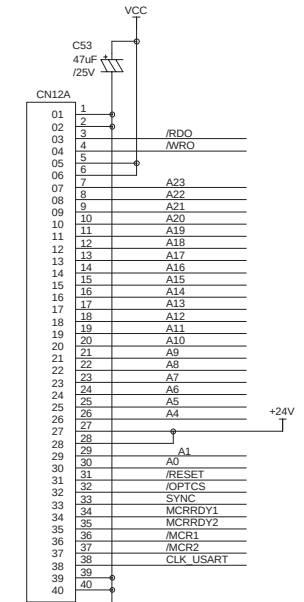
5. INVERTER PWB

1/1



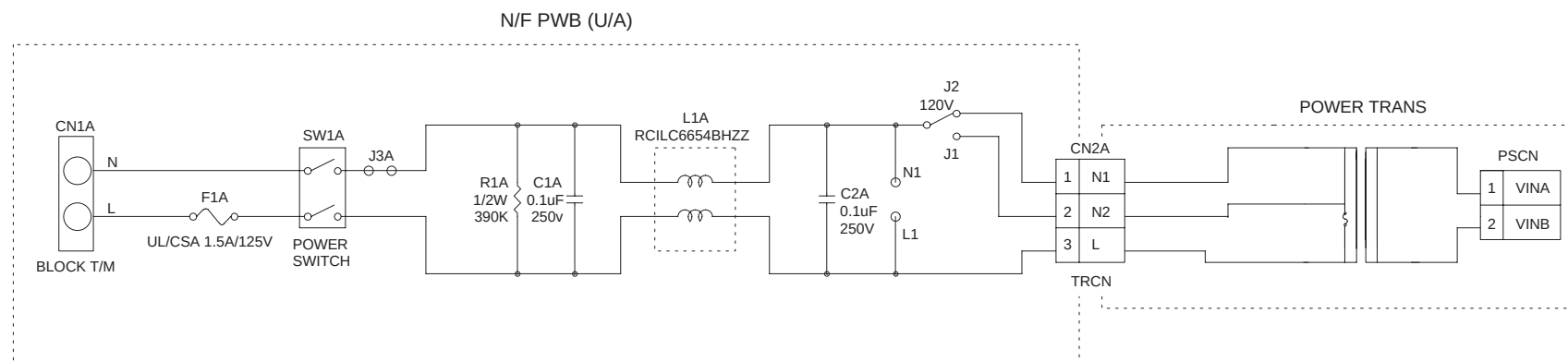
6. MOTHER PWB

1/1



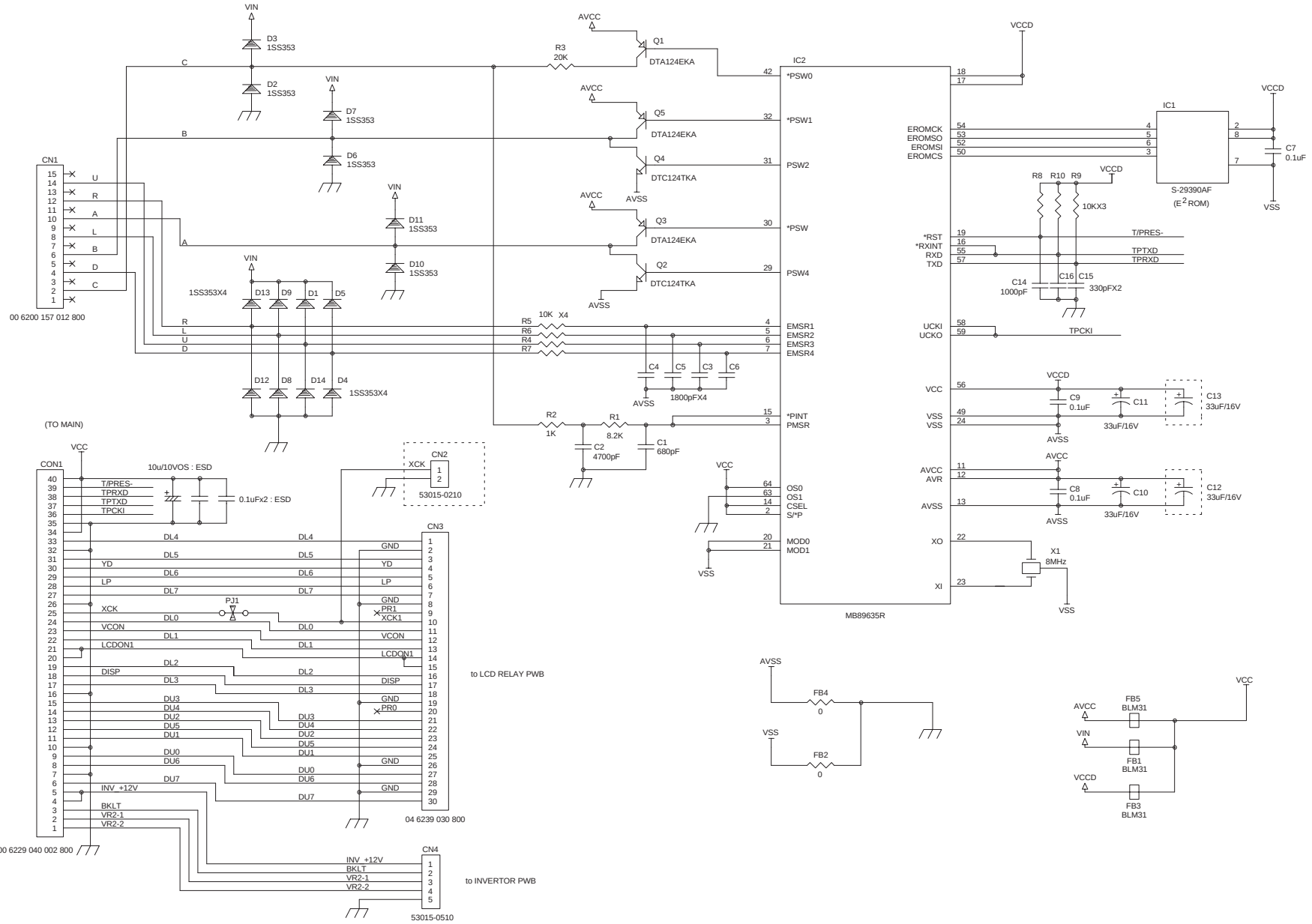
7. N/F PWB UNIT

1/1

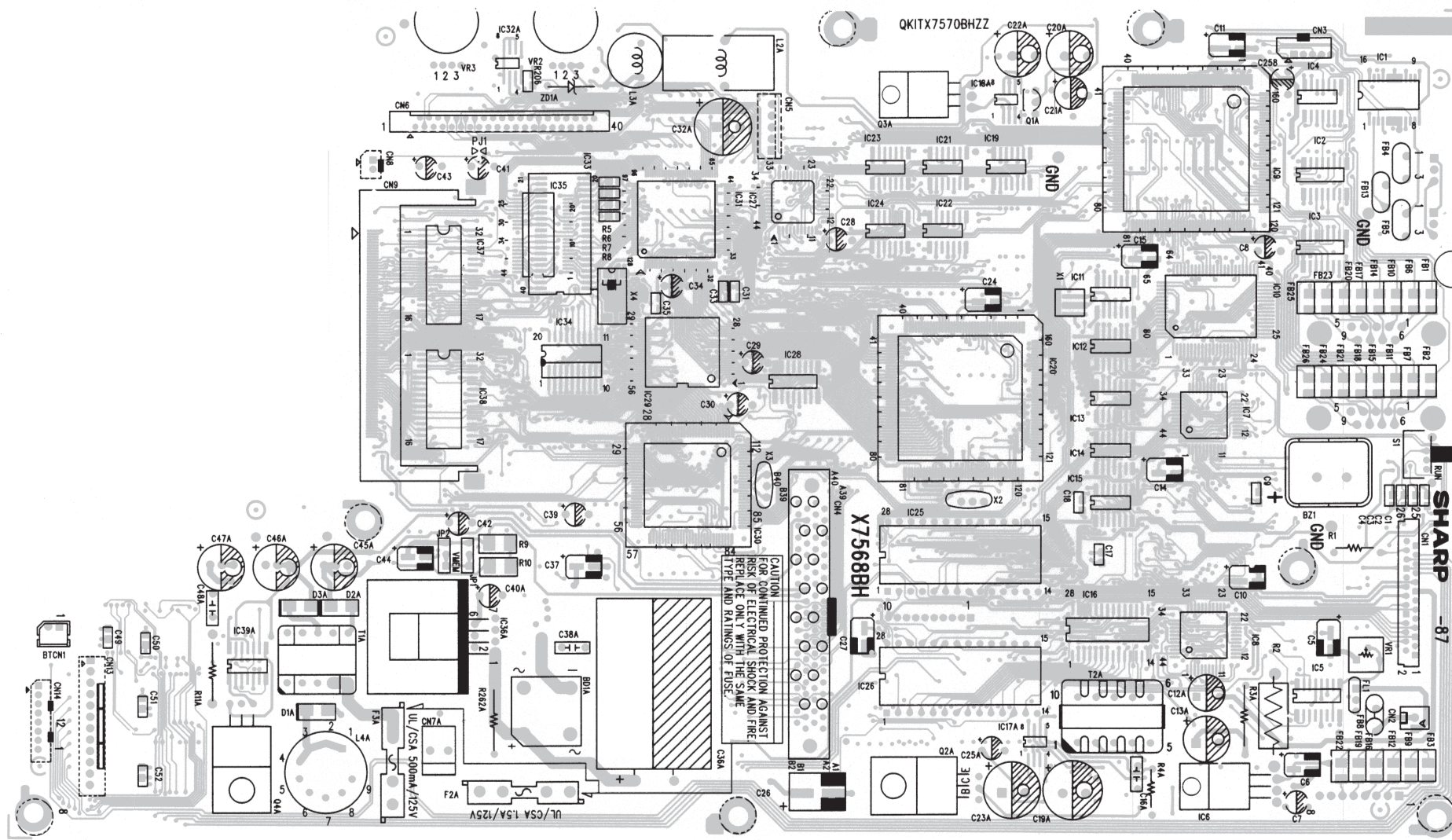


8. TOUCH PANEL PWB

1/1

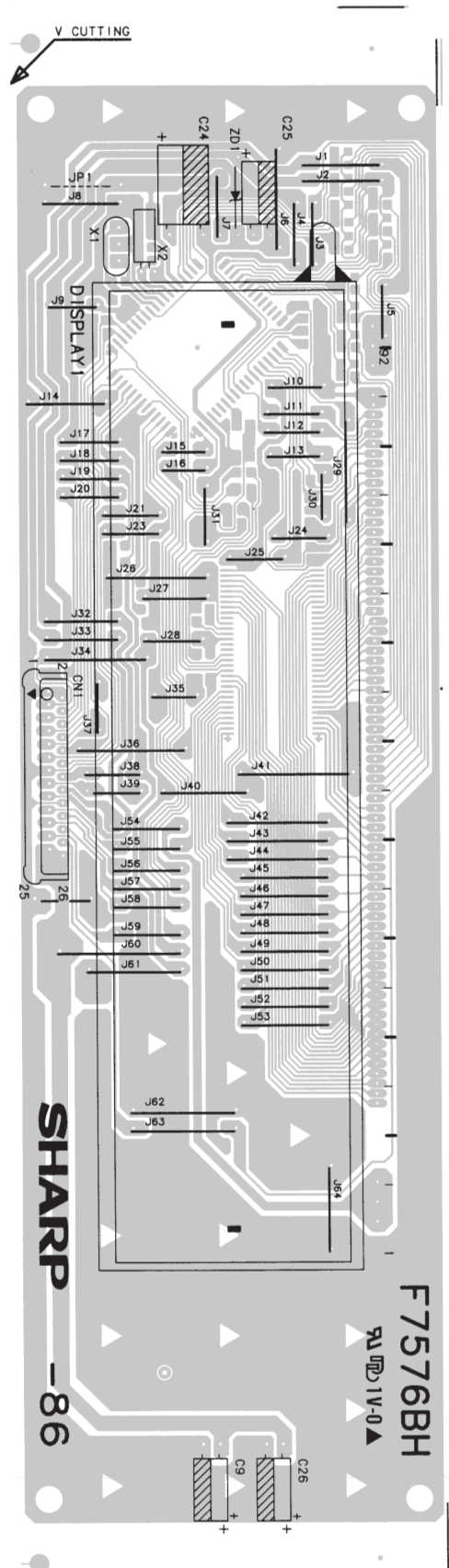


[A side]

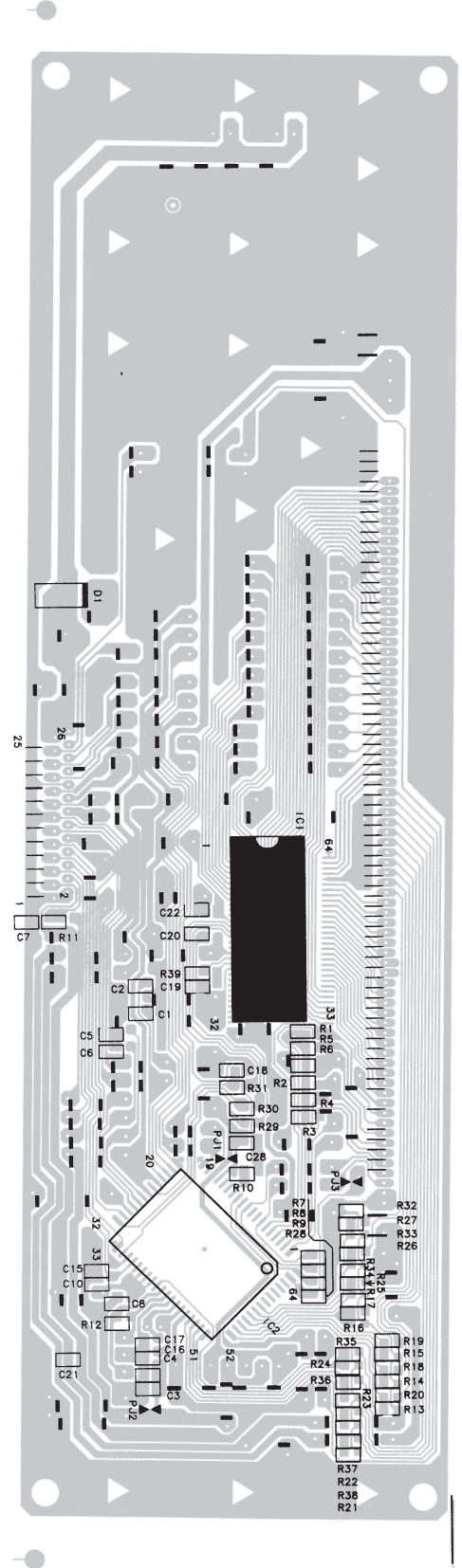


2. CKDC PWB

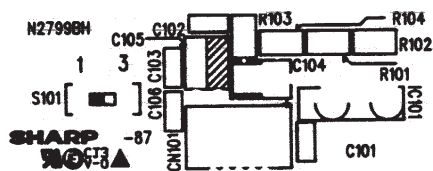
[A side]



[B side]

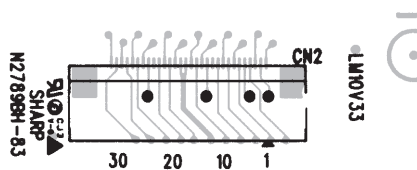


3. IR PWB

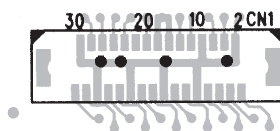


4. LCD PWB

[A side]

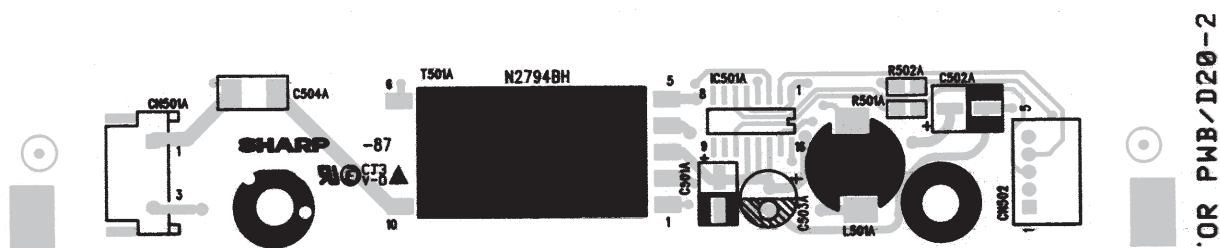


[B side]

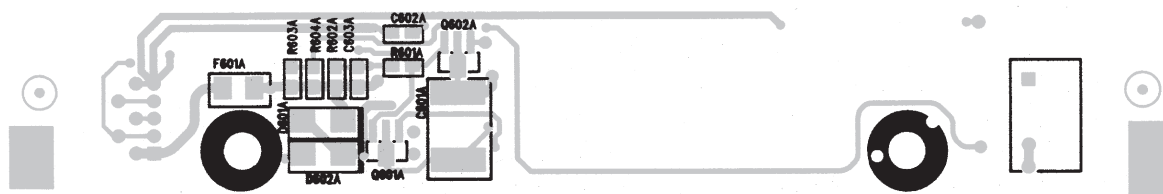


5. INVERTER PWB

[A side]

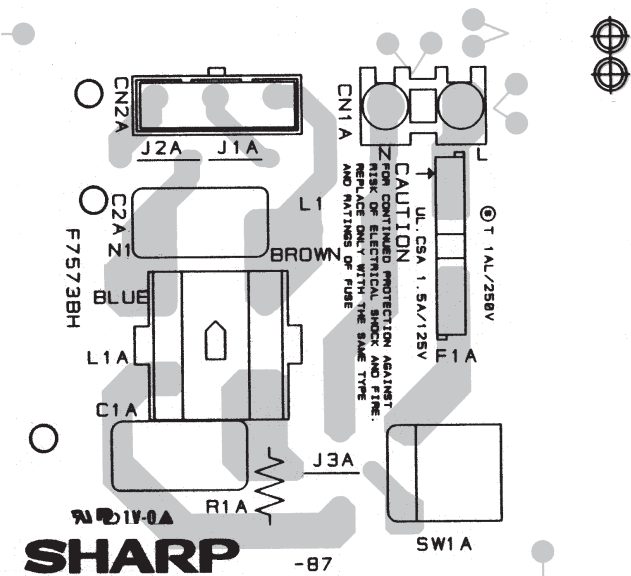
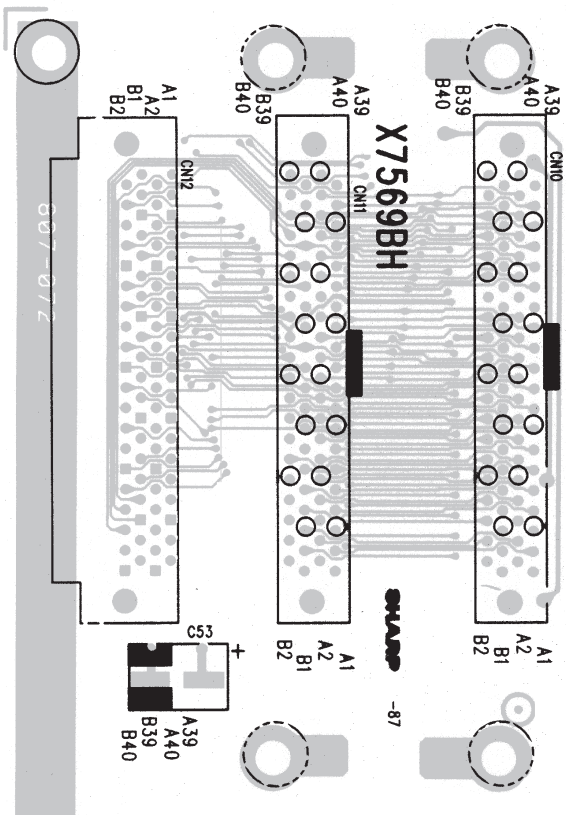


[B side]

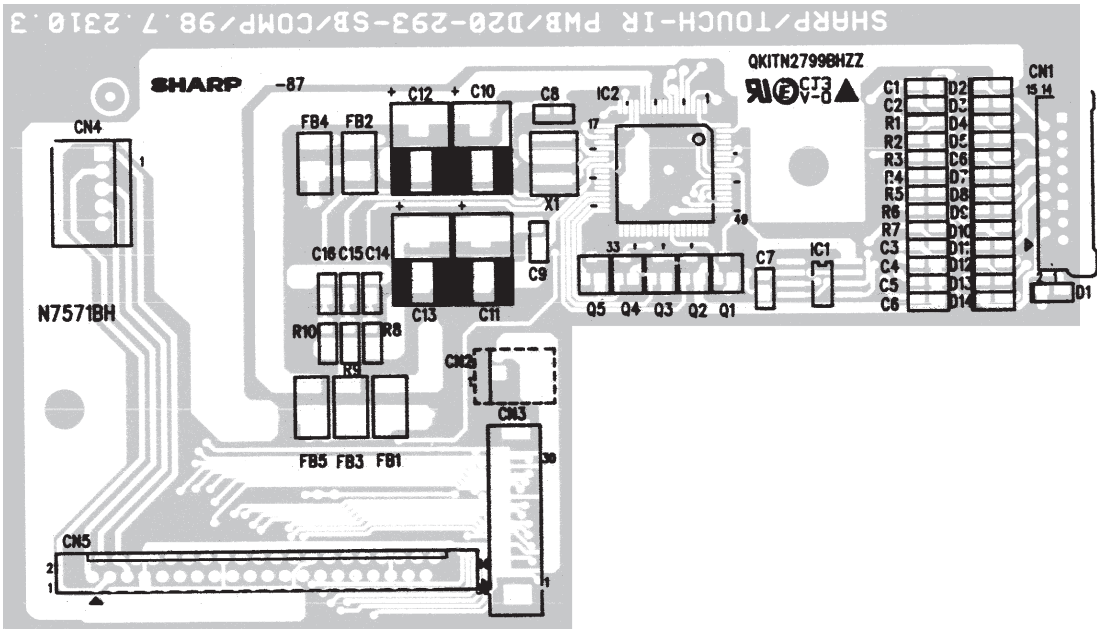


6. MOTER PWB (Side-A)

7. N/F PWB



8. TOUCH PANEL PWB



SHARP PARTS GUIDE

MODEL UP-3300

(for U.S.A., Canada)

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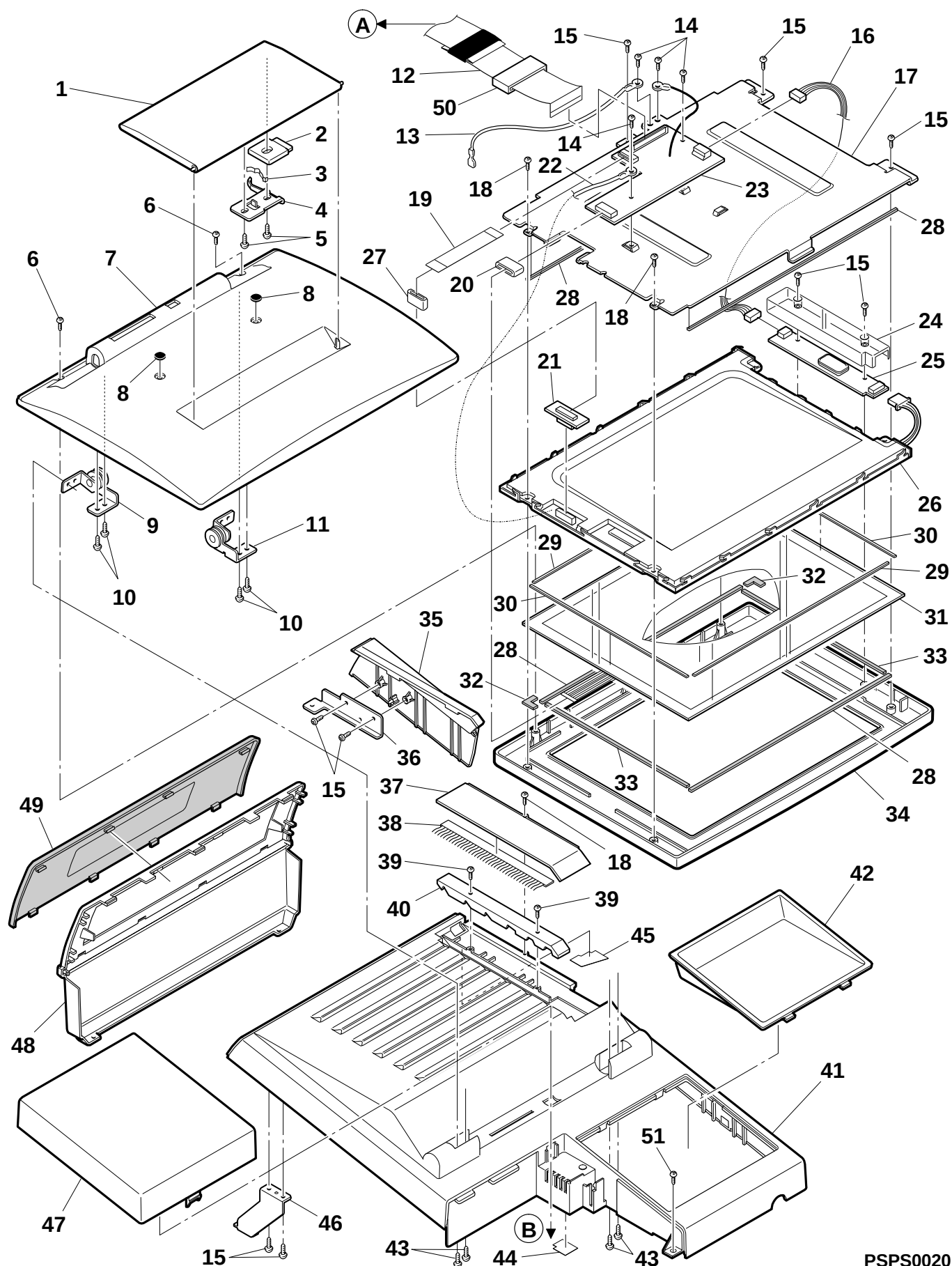
- 1 Top cabinet etc.
- 2 Bottom cabinet etc.
- 3 Packing material & Accessories
- 4 Main PWB unit
- 5 Mother PWB unit
- 6 Touch panel PWB unit
- 7 N/F PWB unit
- 8 Invertor PWB unit
- 9 Rear display PWB unit
- 10 IR PWB unit
- 11 LCD PWB unit
- 12 Service tools
- Index

Because parts marked with "▲" is indispensable for the machine safety maintenance and poeration, it must be replaced with the parts specific to the product specification.

1

[illegible]

1 Top cabinet etc.

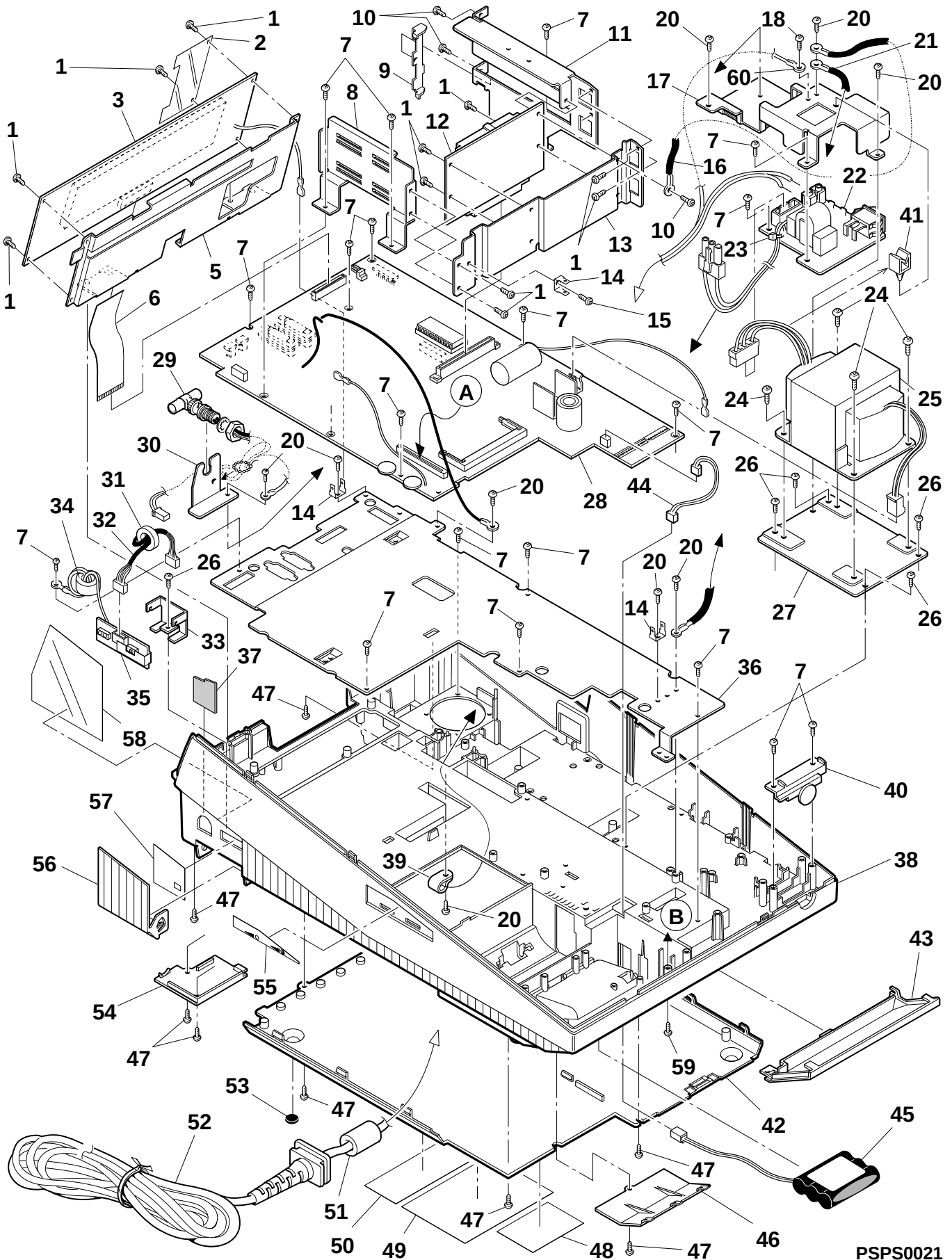


PSPS0020

2 Bottom cabinet etc.

[illegible]

2 Bottom cabinet etc.

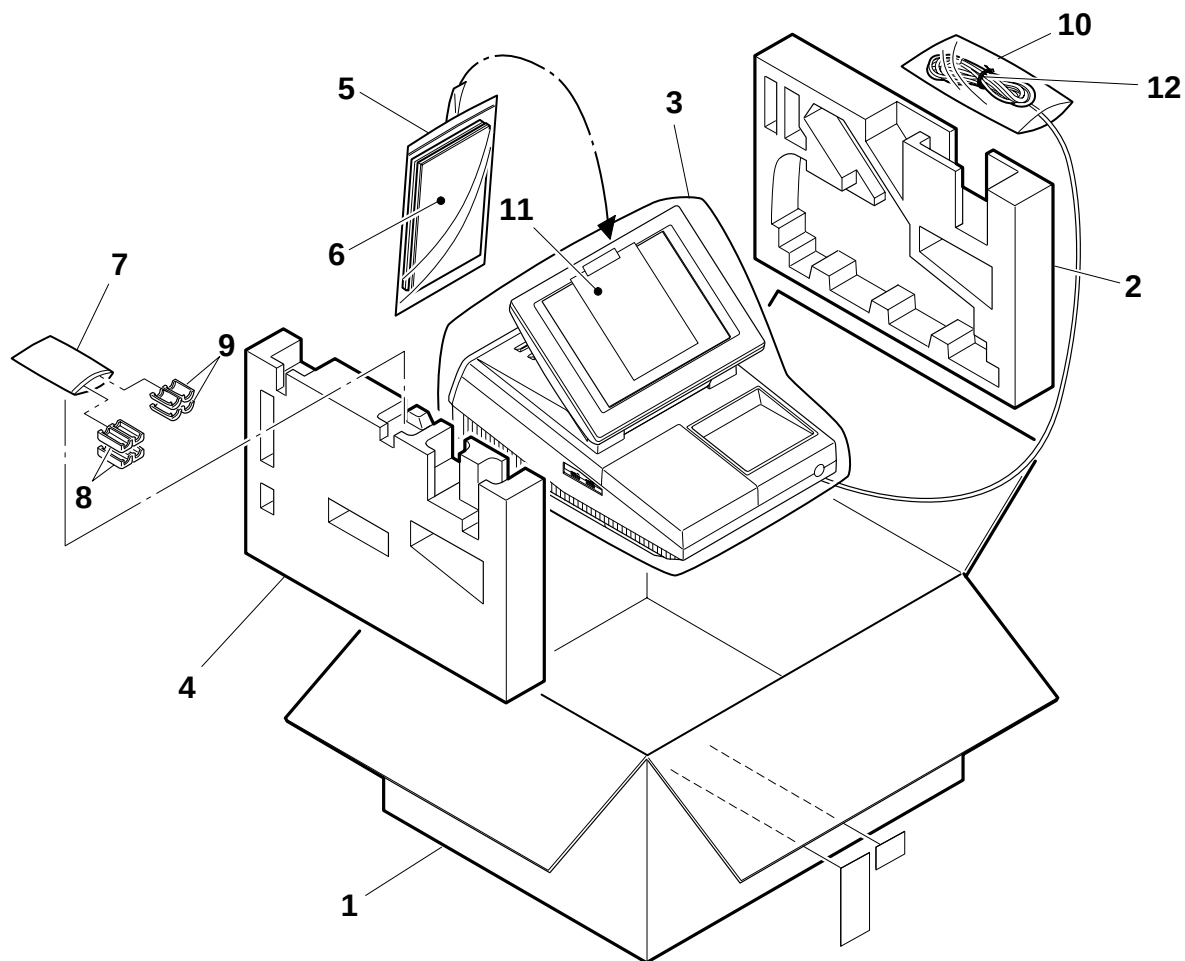


PPS0021

3 Packing material & Accessories

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	SPAKC3019BHZZ	AX	N	D	Packing case [U.S.A]
	SPAKC3020BHZZ	AX	N	D	Packing case [Canada]
2	SPAKA8454BHZZ	AN	N	D	Packing add R
3	SSAKH0003DHZZ	AE		D	Vinyl bag (640×560mm)
4	SPAKA8455BHZZ	AN	N	D	Packing add L
5	SSAKH3015CCZZ	AA		D	Vinyl bag (200×300mm)
6	TINSE7436BHZZ	BK	N	D	Instruction book [U.S.A]
	TINSE7437BHZZ	BK	N	D	Instruction book E [Canada]
	TINSF7438BHZZ	BK	N	D	Instruction book F [Canada]
7	SSAKA5004CCZZ	AA		D	Vinyl bag (100×300mm)
8	RCORF6699BHZZ	AU		C	Core (BNF18)
9	RCORF6700BHZZ	AS		C	Core (BNF-14)
10	SSAKH4231CCZZ	AA		D	Vinyl bag (140×500mm)
11	TCADH6788BHZA	AC		D	Caution card (Black)
12	UBNDA6630BHZZ	AK	N	C	AC cord band

3 Packing material & Accessories



PSPS0022

4 Main PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	QSÖCZ1012AC7B	AP		C	Socket (MM20-72B2-1-T24) [CN9]
2	RCILZ5017SCZ/	AF		C	Chip core (BLM31) [FB1,2,3,6,7,9,10,11,12]
	RCILZ5017SCZ/	AF		C	Chip core (BLM31) [FB14,15,16,17,18,19,20,21]
	RCILZ5017SCZ/	AF		C	Chip core (BLM31) [FB22,23,24,25,26]
3	RCRMZ1016LCZZ	AF		B	Crystal (16MHz(CSTCS16MX040)) [X1]
4	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF) [C31,33,35]
5	VCEAPS1CC106M	AC		C	Capacitor (16WV 10μF) [C5,10,11,14,15,24,27,37,44]
6	VCEAPS1HC104M	AD		C	Capacitor (0.1μF/50V) [C6]
7	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF) [C1,2]
8	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF) [C3,4,9,17,18]
9	VHDSFPB54/-1	AC		B	Diode (SFPB54) [D2A,3A]
10	VHDSFPL52V/-1	AC		B	Diode (SFPL52V) [D1A]
11	VHi2032ARAB1A	AZ	N	B	IC (ISPLS2032B1A) [IC27]
12	VHi28F016SU70	BR		B	IC (16M FROM)(28F016SU70) [IC29]
13	VHi51V8512T12	BG		B	IC (TC51V8512AFT) [IC37,38]
14	VHi74LV138DR/	AP	N	B	IC (74LV138) [IC28]
15	VHi74AHCT245D	AP	N	B	IC (74AHCT245) [IC34]
16	VHi74LVX00/SJ	AL		B	IC (74LVX00) [IC21,22]
17	VHi74LVX32/SJ	AL		B	IC (74LVX32) [IC19,24]
18	VHiBR6265BF10	AR		B	IC (BR6265BF10) [IC16]
19	VHiH641510810	BA		B	IC (H641510810) [IC30]
20	VHiHY514264B6	AW		B	IC (4M DRAM)(HY514264B6) [IC33]
21	VHiBA10339F-1	AD		B	IC (BA10339F) [IC39A]
22	VHiBA10393F-1	AC		B	IC (KIA393F SOP) [IC17A]
23	VHiLZ9FT18/-1	AZ	N	B	IC (LZ9FT18) [IC9]
24	VHiLZ9KF13/-1	BA	N	B	IC (MPC48) [IC20]
25	VHiMB62H149-1	BC		B	IC (MB62H149) [IC10]
26	VHiMC145406F1	AL		B	IC (MC145406F)(VHIMC145406F-) [IC2,3]
27	VHiMC34063AM1	AG		B	IC (MC34063AM1) [IC18A,32A]
28	VHiMN89303/-1	BD		B	IC (MN890303) [IC31]
29	VHiSN74HC00DR	AG		B	IC (74HC00 SOP) [IC12]
30	VHiSN74HC04DR	AG		B	IC (74HC04) [IC13]
31	VHiSN74HC08DR	AL		B	IC (74HC08 SOP) [IC15]
32	VHiSN74HC74D1	AG		B	IC (SN74HC74) [IC14]
33	VHiSN74HCU04D	AG		B	IC (SN74HCU04) [IC11]
34	VHiSN74LS393N	AW		B	IC (74LS393) [IC23]
35	VHiSN75115NS1	AN		B	IC (SN75115NS1) [IC5]
36	VHiSN75189DR/	AK		B	IC (75189) [IC4]
37	VHiTD62308F-1	AH		B	IC (TD62308F) [IC1]
38	VHiZ84C0006FE	AT		B	IC (Z84C0006FE) [IC7]
39	VHiZ84C3006FE	AT		B	IC (Z84C3006FE) [IC8]
40	VRS-TS2AD4330J	AA		C	Resistor (1/10W 33Ω ±5%) [R5,6,7,8]
41	VRS-TS2HD130J	AD	N	C	Resistor (1/2W 13Ω ±5%) [R9,10]
42	RCSRZ2396RCZZ	AL	N	B	X-tal (25.175MHz) [X4]
43	VRS-TS2AD000J	AA		C	Resistor (1/10W 0Ω ±5%) [R206]
44	RCILZ5017SCZ/	AF		C	Chip core (BLM31) [FB33,34,35,36,37,38]
45	RCORF1008ACZZ	AB		C	Chip bead (BUM21A05) [FB27,28,29,30,31,32]
46	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF) [C63,64,68,69,70,71,74,75,77,78]
	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF) [C98,100,102,103,111,114,116,117]
	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF) [C118,119,122,123,127,129,130,132]
	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF) [C133,136,138,140,141,143,145,146]
	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF) [C147,149,151,155,156,157,158,161]
	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF) [C162,164,165,166,171,172,173,174]
	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF) [C175,176,177,178,179,180,181,183]
	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF) [C184,185,186,188,189,190,191,193]
	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF) [C194,195,197,198,199,200,201,202]
	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF) [C203,204,206,208,210,211,213,214]
	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF) [C215,217,218,219,222,224,225,227]
	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF) [C230,233,234,237,240,241,242,247]
	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF) [C248,249,250,251,252,256]
47	VCCCTV1HH8R0J	AC	N	C	Capacitor (50WV 8pF) [C212]
48	VCCCTV1HH100J	AA		C	Capacitor (50WV 10PF) [C209]
49	VCCCTV1HH221J	AA		C	Capacitor (50WV 220PF) [C81,121A,128]
50	VCCCTV1HH331J	AA		C	Capacitor (50WV 330pF) [C66,67,72,73,80,82,85,86,87,88]
	VCCCTV1HH331J	AA		C	Capacitor (50WV 330pF) [C89,90,92,93,95,96,97,99,101,126]
	VCCCTV1HH331J	AA		C	Capacitor (50WV 330pF) [C131,135,137,139,159,160,187,196]
	VCCCTV1HH331J	AA		C	Capacitor (50WV 330pF) [C205,253A,261,262]
51	VCCCTV1HH470J	AA		C	Capacitor (50WV 47PF) [C257]
52	VCCCTV1HH471J	AA		C	Capacitor (50WV 470PF) [C216A]
53	VCKYTV1CF105Z	AB		C	Capacitor (16WV 1μF) [C105,243]
54	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF) [C57,58,60,62,120A,259,260]
55	VCKYTV1HB103K	AB		C	Capacitor (50WV 0.010μF) [C167]
56	VCKYTV1HB152K	AA		C	Capacitor (50WV 1500PF) [C83A,112A]
57	VCKYTV1HB222K	AA		C	Capacitor (50WV 2200PF) [C239A]
58	VCKYTV1HB332K	AA		C	Capacitor (50WV 3300pF) [C65]
59	VCKYTV1HB333K	AA		C	Capacitor (50WV 0.033μF) [C235A]
60	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF) [C61,76,79,84,91,94,104,106,107]
	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF) [C108,109,110,113,115,124A,125,134]
	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF) [C142,144,148,150,152,153,168,169]
	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF) [C170,182,192,207,221,223A,226,231A]

4 Main PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
60	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF) [C238,244,245,246,,220,254,255]
61	VHD1SS353// -1	AB		B	Diode (1SS353) [D4,5,6,7,12,13A,16A,17A,18,19A]
62	VHDSFPB54// -1	AC		B	Diode (SFPB54) [D8A,9,20A,21A]
63	VHDSFPL52V// -1	AC		B	Diode (SFPL52V) [D14A,15A]
64	VHERD30PB// -1	AD		B	Zener diode (RD30PB) [ZD5A]
65	VHERD4.3MB1 -1	AC		B	Zener diode (RD4.3MB1) [ZD3A]
66	VHERD5.6PB// -1	AD		B	Zener diode (RD5.6PB) [ZD4A]
67	VHERD6.2MB1 -1	AC		B	Zener diode (RD6.2MB1) [ZD2A]
68	VHEUDZ33B// -1	AC		B	Zener diode (32.15-33.79)(UDZ33B) [ZD6A]
69	VHi74LV08/DR/	AK	N	B	IC (74LV08) [IC42]
70	VHi74LV14/DR/	AK	N	B	IC (74LV14) [IC44]
71	VHi74LVX08/SJ	AG	N	B	IC (74LVX08) [IC43]
72	VHiRH5RE33A -1	AF		B	IC (RX5RE) [IC45]
73	VHiSN74HC00DR	AG		B	IC (74HC00 SOP) [IC40]
74	VHiUPD71037GB	AY		B	IC (UPD71037GB) [IC41]
75	VHVICPS1.0// -1	AF		B	IC-protector (ICPS1.0) [F3]
76	VRS-TS2AD000J	AA		C	Resistor (1/10W 0Ω ±5%) [R79,146,149]
77	VRS-TS2AD100J	AA		C	Resistor (1/10W 10Ω ±5%) [R100A]
78	VRS-TS2AD101J	AA		C	Resistor (1/10W 100Ω ±5%) [R75A,196,198,203,208,209,213,215]
	VRS-TS2AD101J	AA		C	Resistor (1/10W 100Ω ±5%) [R220,223,225,227,232,236,244,245]
	VRS-TS2AD101J	AA		C	Resistor (1/10W 100Ω ±5%) [R246]
79	VRS-TS2AD102J	AA		C	Resistor (1/10W 1.0KΩ ±5%) [R34,89A,162,184]
80	VRS-TS2AD1032F	AC	N	C	Resistor (1/10W 10.3KΩ ±1%) [R202A]
	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%) [R12,14,15,20,21,22,24,27,35,38]
	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%) [R40,41,45,46,47,48,49,51,52,53]
	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%) [R54,56,57,58,59,60,61,62,63,65]
	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%) [R66,67,68,71,72,73,74,76,80A,82]
	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%) [R83A,91,92,93,95,96,97,98,99,101]
	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%) [R102,103,105,106,107,110,112,113]
	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%) [R114,115,116,117,118,119,120,121]
	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%) [R122,123,124,125,126,127,128,130]
	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%) [R132,134,135,137,139,141,144,147]
	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%) [R150,151,153,154,156,159,165,166]
	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%) [R167,170,171,172,175,176,177,180]
	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%) [R183,185,186,187,190,191,194,199]
	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%) [R200,201,204,207,210,211,212,214]
	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%) [R216,217,218,219,221,222,224,228]
	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%) [R230,231,233,234,237,241,242,243]
	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%) [R247,248,249,255A,258A,263]
82	VRS-TS2AD104J	AA		C	Resistor (1/10W 100KΩ ±5%) [R50A,256A]
83	VRS-TS2AD105J	AA		C	Resistor (1/10W 1MΩ ±5%) [R78,109,197]
84	VRS-TS2AD112J	AA		C	Resistor (1/10W 1.1KΩ ±5%) [R252A]
85	VRS-TS2AD122F	AA		C	Resistor (1/10W 1.2KΩ ±1%) [R108A,205A]
86	VRS-TS2AD122J	AA		C	Resistor (1/10W 1.2KΩ ±5%) [R32]
87	VRS-TS2AD123J	AA		C	Resistor (1/10W 12KΩ ±5%) [R30]
88	VRS-TS2AD132G	AA		C	Resistor (1/10W 1.3KΩ ±2%) [R43A]
89	VRS-TS2AD152G	AA		C	Resistor (1/10W 1.5KΩ ±2%) [R26]
90	VRS-TS2AD152J	AA		C	Resistor (1/10W 1.5KΩ ±5%) [R260A,253A]
91	VRS-TS2AD153J	AA		C	Resistor (1/10W 15KΩ ±5%) [R33,229A]
92	VRS-TS2AD162J	AA		C	Resistor (1/10W 1.6KΩ ±5%) [R37,39]
93	VRS-TS2AD182G	AA		C	Resistor (1/10W 1.8KΩ ±2%) [R44A]
94	VRS-TS2AD183J	AA		C	Resistor (1/10W 18KΩ ±5%) [R235A]
95	VRS-TS2AD220J	AA		C	Resistor (1/10W 22Ω ±5%) [R81A]
96	VRS-TS2AD222J	AA		C	Resistor (1/10W 2.2KΩ ±5%) [R19]
97	VRS-TS2AD223J	AA		C	Resistor (1/10W 22KΩ ±5%) [R239]
98	VRS-TS2AD272J	AA		C	Resistor (1/10W 2.7KΩ ±5%) [R94A]
99	VRS-TS2AD273J	AA		C	Resistor (1/10W 27KΩ ±5%) [R70A]
100	VRS-TS2AD302J	AA		C	Resistor (1/10W 3.0KΩ ±5%) [R42,55]
101	VRS-TS2AD303F	AA		C	Resistor (1/10W 30KΩ ±1%) [R254A]
	VRS-TS2AD330J	AA		C	Resistor (1/10W 33Ω ±5%) [R142,143,152,157,158,160,161,163]
102	VRS-TS2AD330J	AA		C	Resistor (1/10W 33Ω ±5%) [R164,168,169,173,174,178,179,181]
	VRS-TS2AD330J	AA		C	Resistor (1/10W 33Ω ±5%) [R182,188,189,192,193,195]
103	VRS-TS2AD334J	AA		C	Resistor (1/10W 330KΩ ±5%) [R77]
104	VRS-TS2AD362F	AA		C	Resistor (1/10W 3.6KΩ ±1%) [R104A]
105	VRS-TS2AD392G	AA		C	Resistor (1/10W 3.9KΩ ±2%) [R31,88A]
106	VRS-TS2AD432J	AA		C	Resistor (1/10W 4.3KΩ ±5%) [R251A,226A]
107	VRS-TS2AD470J	AA		C	Resistor (1/10W 47Ω ±5%) [R133,136,138,140,145,148]
108	VRS-TS2AD472J	AA		C	Resistor (1/10W 4.7KΩ ±5%) [R13,16,17,23,25,28,129,131,155]
	VRS-TS2AD472J	AA		C	Resistor (1/10W 4.7KΩ ±5%) [R238A,261]
109	VRS-TS2AD472G	AA		C	Resistor (1/10W 4.7KΩ ±2%) [R88A]
110	VRS-TS2AD473J	AA		C	Resistor (1/10W 47KΩ ±5%) [R18]
111	VRS-TS2AD512F	AA		C	Resistor (1/10W 5.1KΩ ±1%) [R257A]
112	VRS-TS2AD513J	AA		C	Resistor (1/10W 51KΩ ±5%) [R259A]
113	VRS-TS2AD561J	AA		C	Resistor (1/10W 560Ω ±5%) [R29]
114	VRS-TS2AD562J	AA		C	Resistor (1/10W 5.6KΩ ±5%) [R86A,69A]
115	VRS-TS2AD563J	AA		C	Resistor (1/10W 56KΩ ±5%) [R87A,90A]
116	VRS-TS2AD622J	AA		C	Resistor (1/10W 6.2KΩ ±5%) [R250A]
117	VRS-TS2AD681J	AA		C	Resistor (1/10W 680Ω ±5%) [R111]
118	VRS-TS2AD682J	AA		C	Resistor (1/10W 6.8KΩ ±5%) [R64A]
119	VRS-TS2AD802J	AC	N	C	Resistor (1/10W 8KΩ ±5%) [R240]

4



5 Mother PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	QCNCM7203RC8J	AN		C	Option connector (20-5061-080) [CN12]
2	QCNCW7204RC8J	AM		C	I/O connector (80PIN;ST 10-5061-080) [CN4,10,11]
3	VCEAPS1EC476M	AF		C	Capacitor (25WV 47μF) [C53]
	(Unit)				
901	CPWBX7569BH01	CA	N	E	Mother PWB unit

6 Touch panel PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	QCNCW7217RC3J	AK		C	Connector (ELCO 04-6239-030-001-800) [CN3]
2	RCiLZ5017SCZ/	AF		C	Chip core (BLM31) [FB1,3,5]
3	RCRMZ7002RCZZ	AE		B	Crystal (8 MHz) [X1]
4	VCCCTV1HH331J	AA		C	Capacitor (50WV 330pF) [C15,16]
5	VCCCTV1HH681J	AA		C	Capacitor (50WV 680PF) [C1]
6	VCEAPS1CC336M	AF		C	Capacitor (16WV 33μF) [C10,11]
7	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF) [C14]
8	VCKYTV1HB182K	AA		C	Capacitor (50WV 1800PF) [C3,4,5,6]
9	VCKYTV1HB472K	AA		C	Capacitor (50WV 4700pF) [C2]
10	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF) [C7,8,9]
11	VHD1SS353// -1	AB		B	Diode (1SS353) [D1,2,3,4,5,6,7,8]
12	VHiM89635N010	BA		B	IC (MB89635R) [IC2]
13	VHiS29390AFJA	AL		B	IC (E2PROM)(S-29390AF) [IC1]
14	VRS-TS2AD102J	AA		C	Resistor (1/10W 1.0KΩ ±5%) [R2]
15	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%) [R4,5,6,7,8,9,10]
16	VRS-TS2AD203J	AA		C	Resistor (1/10W 20KΩ ±5%) [R3]
17	VRS-TS2AD822J	AA		C	Resistor (1/10W 8.2KΩ ±5%) [R1]
18	VSDTA124EK/-1	AD		B	Transistor (DTA124EKA) [Q1,3,5]
19	VSDTC124TK/-1	AD		B	Transistor (DTC124TKA) [Q4,2]
20	VRS-TQ2BB000J	AA		C	Resistor (1/8W 0Ω ±5%) [FB2,4]
21	RC-EZ106ARC1A	AD		C	Capacitor (10WV 10μF) [C26]
22	RC-KZ1054CCZZ	AB		C	Capacitor (50WV 0.1μF) [C24,25]
23	QCNCM7226BH0E	AD		C	Connector (MLX53015-0510) [CN4]
24	QCNCM7230BH1E	AL		C	Connector (00-6200-157-012-800) [CN1]
25	QCNCM7207BH4J	AQ		C	Connector (40P)(6229ZiF DIP) [CON1]
26	QCNW-2994BHZZ	AE	N	C	GND wire
	(Unit)				
901	CPWBN7571BH01	BR	N	E	Touch panel PWB unit

7 N/F PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	VRD-RB2HY394J	AA		C	Resistor (1/2W 390KΩ ±5%) [R1A]
2	QCNCW7199BH0E	AE		C	Connector (35328-0510) [CN2A]
3	QFS-B1039CCZZ	AD		A	Fuse (UL 1.5A/125V) [F1A]
4	QFSHD2109AFZZ	AC		C	Fuse holder (HD2109AF) [F1A]
5	QTANN6658RCZZ	AH		C	Block terminal [CN1A]
6	RC-FZ1041RC2E	AE		C	Capacitor (250WV 0.1μF) [C1A,2A]
7	RCiLC6654BHZZ	AR		C	Coil (5021C) [L1A]
8	QCNW-2982BHZZ	AN	N	B	AC cable [L1,N1]
9	QSW-C1262QCZZ	AR		B	Power switch (AJ7241B) [SW1A]
10	LBNDJ2003SCZZ	AA		C	Cable band
	(Unit)				
901	CPWBF7573BH01	BG	N	E	N/F PWB unit

8 Invertor PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	QCNCM2656RC0C	AE		C	Connector (BHR-03VS-1) [CN501A]
2	RC-CZ2201RC0F	AE		C	Capacitor (22pF/3.15KV) [C504A]
3	RCiLC6667BHZZ	AN		C	Coil (100μH SMD) [L501A]
4	RTRNH9521BHZZ	BB		B	Transformer (841TN-1157) [T501A]
5	VHiLT1184CS-1	BE		B	IC (LT1184) [IC501A]
6	VCEAPS1CC225M	AF		C	Capacitor (2.2μF/16V) [C501A]
7	VCEAPS1CC226M	AC		C	Capacitor (16WV 22μF) [C502A]
8	VRS-TS2AD133F	AA		C	Resistor (1/10W 13KΩ ±1%) [R501A]
9	VRS-TS2AD472J	AA		C	Resistor (1/10W 4.7KΩ ±5%) [R502A]
10	RC-FZ8231RC2A	AG		C	Capacitor (0.082μF/100V) [C601A]
11	VCKYTV1CF105Z	AB		C	Capacitor (16WV 1μF) [C602A]

8 Invertor PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
12	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF) [C103]
13	VHDSFPB54/-1	AC		B	Diode (SFPB54) [D601A,602A]
14	VHV iCPS0.5/-1	AF		B	IC-protector (ICPS0.5) [F601A]
15	VRS-TS2AD104J	AA		C	Resistor (1/10W 100KΩ ±5%) [R601A]
16	VRS-TS2AD222J	AA		C	Resistor (1/10W 2.2KΩ ±5%) [R603A,604A]
17	VRS-TS2AD224J	AA		C	Resistor (1/10W 220KΩ ±5%) [R602A]
18	VS2SD2391/-1	AD		B	Transistor (2SD2391Q) [Q601A,602A]
19	QCNCM7226BH0E	AD		C	Connector (MLX53015-0510) [CN502]
	(Unit)				
901	CPWBN2794BH01	BQ	N	E	Inverter PWB unit

9 Rear display PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	VH iH4728B02FS	AW	N	B	IC (H4728B02FS) [IC2]
2	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF) [C19]
3	VCCCTV1HH150J	AA		C	Capacitor (50WV 15PF) [C16,17]
4	VCCCTV1HH471J	AA		C	Capacitor (50WV 470PF) [C1,5,6,7,10,15,18,28]
5	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF) [C2]
6	VCKYTV1HB222K	AA		C	Capacitor (50WV 2200PF) [C22]
7	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF) [C3,4,8,20,21]
8	VHDSFPB54/-1	AC		B	Diode (SFPB54) [D1]
9	VH iM66004FP-1	AY		B	IC (M66004FP) [IC1]
10	VRS-TS2AD104J	AA		C	Resistor (1/10W 100KΩ ±5%) [R1,2,3,4,5,6,7,8]
	VRS-TS2AD104J	AA		C	Resistor (1/10W 100KΩ ±5%) [R9,13,14,15,16,21]
	VRS-TS2AD104J	AA		C	Resistor (1/10W 100KΩ ±5%) [R22,23,24,25,26,27]
	VRS-TS2AD104J	AA		C	Resistor (1/10W 100KΩ ±5%) [R28]
11	VRS-TS2AD105J	AA		C	Resistor (1/10W 1MΩ ±5%) [R12]
12	VRS-TS2AD202J	AA		C	Resistor (1/10W 2KΩ ±5%) [R17,18,19,20,32,33]
	VRS-TS2AD202J	AA		C	Resistor (1/10W 2KΩ ±5%) [R34,35,36,37,38]
13	VRS-TS2AD273G	AC		C	Resistor (1/10W 27KΩ ±2%) [R39]
14	VRS-TS2AD330J	AA		C	Resistor (1/10W 33Ω ±5%) [R11,29,30,31]
15	VRS-TS2AD473J	AA		C	Resistor (1/10W 47KΩ ±5%) [R10]
16	VHERD39EB7/-1	AB		B	Zener diode (RD39EB7) [ZD1]
17	PSPAG6729RCZZ	AF	N	C	Display gum
18	QCNCW7195RC2F	AN		C	Connector (26pin) [CN1]
19	RCRSP6676RCZZ	AG		B	Crystal (DT38 32.768KHz) [X2]
20	RCRSZ6644RCZZ	AD		B	Crystal (4.19MHz) [X1]
21	VCEAEU1CW106M	AA		C	Capacitor (16WV 10μF) [C9,24,25,26]
22	VVK112-LT04GK	BQ	N	B	Display tube (112-LT-04GK) [DISPLAY TUBE]
23	QCNCW-2990BHZZ	AP	N	C	GND wire
	(Unit)				
901	CPWBF7576BH01	BV	N	E	Rear-Disp PWB unit

10 IR PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	VCCCTV1HH331J	AA		C	Capacitor (50WV 330pF) [C106]
2	VCEAPS1CC475M	AG	N	C	Capacitor (4.7μF/16V) [C104]
3	VCKYTV1HB333K	AA		C	Capacitor (50WV 0.033μF) [C101]
4	VCKYTV1HB334K	AE		C	Capacitor (50WV 0.33μF) [C102]
5	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF) [C103]
6	VHPRPM851/-1	AT		B	Photo coupler (RPM851) [IC101]
7	VRS-TQ2BB331J	AA		C	Resistor (1/8W 330Ω ±5%) [R104]
8	VRS-TQ2BB340J	AB	N	C	Resistor (1/8W 34Ω ±5%) [R101,102]
9	VRS-TQ2BB470J	AB	N	C	Resistor (1/8W 47Ω ±5%) [R103]
10	QSW-S2403BHZZ	AW	N	B	SL-switch [S101]
11	QCNCM7226BH0E	AD		C	Connector (MLX53015-0510) [CN101]
12	RC-EZ106ARC1A	AD		C	Capacitor (10WV 10μF) [C105]
13	LANGQ7648BHZZ	AG	N	C	IR slide plate
14	QCNCW-2994BHZZ	AE	N	C	GND wire
	(Unit)				
901	CPWBN2799BH01	BN	N	E	IR PWB unit

11 LCD PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	QCNCW7217RC3J	AK		C	Connector (30pin)(04-6239-030-001-800) [CN2]
2	QCNCW1230AC3A	AK		C	Connector (31pin) [CN1]
	(Unit)				
901	CPWBN2789BH01	BA		E	LCD PWB unit

12 Service tools

[illegible]

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PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
【C】					
CKÖG-6724BHZZ	12- 4	BQ		S	
CPWBF7573BH01	2- 22	BG	N	E	
"	7-901	BG	N	E	
CPWBF7576BH01	2- 3	BV	N	E	
"	9-901	BV	N	E	
CPWBN2789BH01	1- 21	BA		E	
"	11-901	BA		E	
CPWBN2794BH01	1- 25	BQ	N	E	
"	8-901	BQ	N	E	
CPWBN2799BH01	2- 35	BN	N	E	
"	10-901	BN	N	E	
CPWBN7571BH01	1- 23	BR	N	E	
"	6-901	BR	N	E	
CPWBX7568BH01	2- 28	DB	N	E	
"	4-901	DB	N	E	
CPWBX7569BH01	2- 12	CA	N	E	
"	5-901	CA	N	E	
【G】					
GCABA7871BHZZ	2- 38	BF	N	D	
GCABB7870BHZZ	1- 41	BB	N	D	
GCABE7872BHZZ	1- 34	AX	N	D	
GCABF7873BHZZ	1- 7	BA	N	D	
GCOVA7131BHSS	2- 40	AH	N	D	
GCOVA7158BHZZ	1- 48	AW	N	D	
GCOVA7159BHZZ	1- 35	AS	N	D	
GCOVA7166BHZZ	1- 37	AP	N	D	
GCOVH2472BHZZ	2- 42	BA	N	D	
GCOVH7160BHZZ	2- 46	AN	N	D	
GCOVH7161BHZZ	2- 56	AN	N	D	
GCOVH7167BHZZ	1- 24	AH	N	D	
GFTAT6927BHZZ	1- 42	AR	N	D	
GFTAT6928BHZZ	1- 47	AV	N	D	
GFTAU2426BHZZ	2- 43	AR	N	D	
GLEGG6656BHZZ	2- 53	AF		D	
GSTN-2005BHZZ	1- 1	AT	N	C	
【H】					
HPNLC6839RCZZ	1- 31	BT		D	
【J】					
JKNBZ2411BHZZ	1- 2	AH	N	C	
JKNBZ6923BHZZ	1- 40	AP	N	C	
【L】					
LANGK2805BHZZ	2- 27	AQ	N	C	
LANGK2807BHZZ	2- 33	AQ	N	C	
LANGK7649BHZZ	1- 17	AV	N	C	
LANGK7650BHZZ	1- 46	AH	N	C	
LANGK7651BHZZ	1- 36	AL	N	C	
LANGQ7648BHZZ	10- 13	AG	N	C	
LANGT2808BHZZ	2- 9	AK	N	C	
LANGT7637BHZZ	2- 11	AT	N	C	
LANGT7638BHZZ	2- 8	AM	N	C	
LANGT7639BHZZ	2- 30	AH	N	C	
LANGT7640BHZZ	2- 13	AR	N	C	
LANGT7641BHZZ	2- 17	AR	N	C	
LANGT7658BHZZ	2- 5	AP	N	C	
LBNDJ2003SCZZ	2- 23	AA		C	
"	7- 10	AA		C	
LCHSM6709BHZZ	2- 36	AX	N	C	
LHLDK6847BHZZ	2- 54	AN	N	C	
LHLDW0006SCZZ	2- 39	AB		C	
LHLDW2365BHZZ	2- 41	AG	N	C	
LX-BZ6778BHZZ	2- 10	AA		C	
LX-BZ6782BHZZ	2- 1	AA		C	
LX-BZ6787BHZZ	1- 5	AB		C	
【M】					
MHNG-2324BHZZ	1- 9	AX	N	C	
MHNG-2325BHZZ	1- 11	AX	N	C	
MLEVF2324BHZZ	1- 4	AG	N	C	
MSPRP2372BHZZ	1- 3	AE	N	C	
【P】					
PFiLW2423BHZZ	2- 37	AP	N	D	
PFiLW6979BHZZ	1- 49	AV	N	D	
PGUMM2389BHZZ	1- 8	AE	N	C	
PGUMM6730BHZZ	1- 33	AS		C	
PGUMM6731BHZZ	1- 28	AR		C	
PGUMM6732BHZZ	1- 30	AS		C	
PGUMM6733BHZZ	1- 29	AR		C	
PGUMM6734BHZZ	1- 32	AL		C	
PRDAF6667BHZZ	4-143	AH		C	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
PSHEG2859BHZZ	1- 38	AV	N	C	
PSHEP2471BHZZ	1- 45	AH	N	C	
PSHEP2472BHZZ	1- 44	AH	N	C	
PSHEP2860BHZZ	2- 2	AR	N	C	
PSHEP2861BHZZ	2- 57	AH	N	C	
PSHEP2862BHZZ	2- 58	AH	N	C	
PSPAG6729RCZZ	9- 17	AF	N	C	
【Q】					
QACCD8411BHZZ	2- 52	AV		B	
QCNCM1101BHZZ	4-144	AC		C	
QCNCM2656RC0C	8- 1	AE		C	
QCNCM2788BH0 i	4-186	BL	N	C	
QCNCM7057BH08	4-187	AG		C	
QCNCM7057BHZZ	4-188	AB		C	
QCNCM7075BH0B	4-145	AB		C	
QCNCM7145RCZZ	12- 1	AZ		S	
QCNCM7176BH0E	4-146	AC		C	
QCNCM7176BH1 J	4-189	AD		C	
QCNCM7183BH2F	4-147	AR		C	
QCNCM7203RC8 J	5- 1	AN		C	
QCNCM7207BH4 J	4-148	AQ		C	
"	6- 25	AQ		C	
QCNCM7226BH0E	6- 23	AD		C	
"	8- 19	AD		C	
"	10- 11	AD		C	
QCNCM7230BH1E	6- 24	AL		C	
QCNCW1230AC3A	11- 2	AK		C	
QCNCW7081BHZZ	4-149	AB		C	
QCNCW7195RC2F	9- 18	AN		C	
QCNCW7199BH0E	7- 2	AE		C	
QCNCW7204RC8 J	4-150	AM		C	
"	5- 2	AM		C	
QCNCW7217RC3 J	6- 1	AK		C	
"	11- 1	AK		C	
QCNW-2972BHZZ	1- 12	AU	N	C	
QCNW-2973BHZZ	1- 19	AS	N	C	
QCNW-2974BHZZ	2- 6	AP	N	C	
QCNW-2975BHZZ	2- 32	AY	N	C	
QCNW-2976BHZZ	1- 16	AK	N	C	
QCNW-2978BHZZ	2- 29	BK	N	C	
QCNW-2982BHZZ	7- 8	AN	N	B	
QCNW-2989BHZZ	4-183	AF	N	C	
QCNW-2990BHZZ	4-184	AG	N	C	
"	9- 23	AP	N	C	
QCNW-2991BHZZ	4-185	AH	N	C	
QCNW-2992BHZZ	2- 16	AF	N	C	
QCNW-2993BHZZ	2- 21	AG	N	C	
QCNW-2994BHZZ	6- 26	AE	N	C	
"	10- 14	AE	N	C	
QCNW-2995BHZZ	1- 13	AF	N	C	
QCNW-2996BHZZ	1- 22	AD	N	C	
QCNW-7708BHZZ	2- 44	AM		C	
QFS-B1039CCZZ	4-151	AD		A	
"	7- 3	AD		A	
QFS-C5012CCZZ	4-152	AF		A	
QFSHD2109AFZZ	4-127	AC		C	
"	7- 4	AC		C	
QSÖCZ1012AC7B	4- 1	AP		C	
QSÖCZ6428ACZZ	4-153	AE		C	
QSW-C1262QCZZ	7- 9	AR		B	
QSW-S2403BHZZ	10- 10	AW	N	B	
QSW-S6894BHZZ	4-154	AK		B	
QTANN6658RCZZ	7- 5	AH		C	
QTANP0004BHZA	2- 60	AE		C	
QTANZ6661BHZZ	2- 14	AE		C	
【R】					
RALMB6640RCZZ	4-155	AF		B	
RC-CZ2201RC0F	8- 2	AE		C	
RC-EZ106ARC1A	4-128	AD		C	
"	6- 21	AD		C	
"	10- 12	AD		C	
RC-EZ2271RC1A	4-156	AM		C	
RC-EZ336ARC1A	4-157	AB		C	
RC-FZ1041RC2E	7- 6	AE		C	
RC-FZ8231RC2A	8- 10	AG		C	
RC-KZ1054CCZZ	6- 22	AB		C	
RCiLC6647BHZZ	4-158	AK		C	
RCiLC6652RCZZ	4-159	AK		C	
RCiLC6653BHZZ	4-160	AS		C	
RCiLC6654BHZZ	7- 7	AR		C	
RCiLC6667BHZZ	8- 3	AN		C	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
RCiLZ1003BHZZ	4-129	AF		C	
RCiLZ5017SCZ/	4- 2	AF		C	
"	4- 44	AF		C	
"	6- 2	AF		C	
RCORF1008ACZZ	4- 45	AB		C	
RCORF2025HCZZ	1- 20	AL		C	
RCORF2031SCZZ	1- 50	AN		C	
RCORF6691BHZZ	4-130	AD		C	
RCORF6695BHZZ	2- 51	AK		C	
RCORF6697BHZZ	2- 31	AF		C	
RCORF6698BHZZ	2- 34	AR		C	
RCORF6699BHZZ	3- 8	AU		C	
RCORF6700BHZZ	3- 9	AS		C	
RCORF6702BHZZ	4-131	AF		C	
RCORF6709RCZZ	1- 27	AL		C	
RCRMZ1016LCZZ	4- 3	AF		B	
RCRMZ7002RCZZ	6- 3	AE		B	
RCRSP5019BCZZ	4-132	AD		B	
RCRSP6664RCZZ	4-161	AF		B	
RCRSP6676RCZZ	9- 19	AG		B	
RCRSZ2396RCZZ	4- 42	AL	N	B	
RCRSZ6644RCZZ	9- 20	AD		B	
RTRNH6783RCZZ	4-162	AN		B	
RTRNH6894RCZZ	4-163	AU		B	
RTRNH9521BHZZ	8- 4	BB		B	
RTRNP2402BHZZ	2- 25	BL	N	B	
RVR-B5310QCZ3	4-190	AG		B	
RVR-M2415QCNC3	4-164	AE		B	
【S】					
SPAKA8454BHZZ	3- 2	AN	N	D	
SPAKA8455BHZZ	3- 4	AN	N	D	
SPAKC3019BHZZ	3- 1	AX	N	D	
SPAKC3020BHZZ	3- 1	AX	N	D	
SSAKA5004CCZZ	3- 7	AA		D	
SSAKH0003DHZZ	3- 3	AE		D	
SSAKH3015CCZZ	3- 5	AA		D	
SSAKH4231CCZZ	3- 10	AA		D	
【T】					
TCADH6788BHZA	3- 11	AC		D	
TCAUZ6685BHZA	2- 50	AA		D	
TCAUZ6687BHZA	2- 50	AF		D	
TiNSE7436BHZZ	3- 6	BK	N	D	
TiNSE7437BHZZ	3- 6	BK	N	D	
TiNSF7438BHZZ	3- 6	BK	N	D	
TLABG6967BHZZ	2- 48	AC		D	
TLABG7097BHZZ	2- 49	AF		D	
TLABH2460BHZZ	2- 55	AE	N	D	
【U】					
UBATN2338RCZZ	2- 45	BE	N	B	
UBNDA6630BHZZ	3- 12	AK	N	C	
UKOG-6705RCZZ	12- 3	BC		S	
UKOG-6718RCZZ	12- 2	BE		S	
【V】					
VCCCTV1HH100J	4- 48	AA		C	
VCCCTV1HH101J	4- 4	AA		C	
"	4- 46	AA		C	
"	9- 2	AA		C	
VCCCTV1HH150J	9- 3	AA		C	
VCCCTV1HH221J	4- 49	AA		C	
VCCCTV1HH331J	4- 50	AA		C	
"	6- 4	AA		C	
"	10- 1	AA		C	
VCCCTV1HH470J	4- 51	AA		C	
VCCCTV1HH471J	4- 52	AA		C	
"	9- 4	AA		C	
VCCCTV1HH681J	6- 5	AA		C	
VCCCTV1HH8R0J	4- 47	AC	N	C	
VCEAEU1CW106M	4-133	AA		C	
"	9- 21	AA		C	
VCEAGA1HW105M	4-134	AB		C	
VCEAGA1HW107M	4-135	AA		C	
VCEAGA1HW224M	4-136	AA		C	
VCEAGA1HW475M	4-137	AA		C	
VCEAGU1CW108M	4-165	AD		C	
VCEAGU1HW227M	4-166	AC		C	
VCEAGU1HW477M	4-167	AD		C	
VCEAGU1JW228M	4-168	AV		C	
VCEAGU2AW226M	4-138	AB		C	
VCEAPS1CC106M	4- 5	AC		C	
VCEAPS1CC225M	8- 6	AF		C	
VCEAPS1CC226M	8- 7	AC		C	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
VCEAPS1CC336M	6- 6	AF		C	
VCEAPS1CC475M	10- 2	AG	N	C	
VCEAPS1EC476M	4-191	AF		C	
"	5- 3	AF		C	
VCEAPS1HC104M	4- 6	AD		C	
VCKYTV1CF105Z	4- 53	AB		C	
"	8- 11	AB		C	
VCKYTV1HB102K	4- 7	AA		C	
"	4- 54	AA		C	
"	6- 7	AA		C	
"	8- 12	AA		C	
"	9- 5	AA		C	
VCKYTV1HB103K	4- 55	AB		C	
VCKYTV1HB152K	4- 56	AA		C	
VCKYTV1HB182K	6- 8	AA		C	
VCKYTV1HB222K	4- 57	AA		C	
"	9- 6	AA		C	
VCKYTV1HB332K	4- 58	AA		C	
VCKYTV1HB333K	4- 59	AA		C	
"	10- 3	AA		C	
VCKYTV1HB334K	10- 4	AE		C	
VCKYTV1HB472K	6- 9	AA		C	
VCKYTV1HF104Z	4- 8	AA		C	
"	4- 60	AA		C	
"	6- 10	AA		C	
"	9- 7	AA		C	
"	10- 5	AA		C	
VCQYNA2AM103K	4-139	AA		C	
VCQYNU1HM153K	4-140	AA		C	
VCQYNU1HM683K	4-141	AB		C	
VHD1SS353/-1	4- 61	AB		B	
"	6- 11	AB		B	
VHDCP301///-1	4-169	AL		B	
VHDSFPB54/-1	4- 9	AC		B	
"	4- 62	AC		B	
"	8- 13	AC		B	
"	9- 8	AC		B	
VHDSFPL52V/-1	4- 10	AC		B	
"	4- 63	AC		B	
VHEMTZ13C/-1	4-170	AD	N	B	
VHERD30PB/-1	4- 64	AD		B	
VHERD39EB7/-1	9- 16	AB		B	
VHERD4.3MB1-1	4- 65	AC		B	
VHERD5.6PB/-1	4- 66	AD		B	
VHERD6.2MB1-1	4- 67	AC		B	
VHEUDZ33B/-1	4- 68	AC		B	
VHi2032ARAB1A	4- 11	AZ	N	B	
VHi27256RDH1A	4-174	AW		B	
VHi28F016SU70	4- 12	BR		B	
VHi51V8512T12	4- 13	BG		B	
VHi74AHCT245D	4- 15	AP	N	B	
VHi74LV08/DR/	4- 69	AK	N	B	
VHi74LV138DR/	4- 14	AP	N	B	
VHi74LV14/DR/	4- 70	AK	N	B	
VHi74LVX00/SJ	4- 16	AL		B	
VHi74LVX08/SJ	4- 71	AG	N	B	
VHi74LVX32/SJ	4- 17	AL		B	
VHiBA10339F-1	4- 21	AD		B	
VHiBA10393F-1	4- 22	AC		B	
VHiBR6265BF10	4- 18	AR		B	
VHiH4728B02FS	9- 1	AW	N	B	
VHiH641510810	4- 19	BA		B	
VHiHY514264B6	4- 20	AW		B	
VHiKiA7806P-1	4-171	AK		B	
VHiL4960///-1	4-172	AM		B	
VHiLT1184CS-1	8- 5	BE		B	
VHiLZ9FT18/-1	4- 23	AZ	N	B	
VHiLZ9KF13/-1	4- 24	BA	N	B	
VHiM66004FP-1	9- 9	AY		B	
VHiM89635N010	6- 12	BA		B	
VHiMB62H149-1	4- 25	BC		B	
VHiMC145406F1	4- 26	AL		B	
VHiMC34063AM1	4- 27	AG		B	
VHiMC68B54/-1	4-173	BB		B	
VHiMN89303/-1	4- 28	BD		B	
VHiRH5RE33A-1	4- 72	AF		B	
VHiS29390AFJA	6- 13	AL		B	
VHiSN74HC00DR	4- 29	AG		B	
"	4- 73	AG		B	
VHiSN74HC04DR	4- 30	AG		B	
VHiSN74HC08DR	4- 31	AL		B	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
VHiSN74HC74D1	4- 32	AG		B	
VHiSN74HCU04D	4- 33	AG		B	
VHiSN74LS393N	4- 34	AW		B	
VHiSN75115NS1	4- 35	AN		B	
VHiSN75189DR/	4- 36	AK		B	
VHiTD62308F-1	4- 37	AH		B	
VHiUPD71037GB	4- 74	AY		B	
VHiZ84C0006FE	4- 38	AT		B	
VHiZ84C3006FE	4- 39	AT		B	
VHPRPM851///-1	10- 6	AT		B	
VHViCPS0.5/-1	8- 14	AF		B	
VHViCPS1.0/-1	4- 75	AF		B	
VRD-RB2HY394J	7- 1	AA		C	
VRD-RC2EY221J	4-175	AA		C	
VRD-RC2EY392G	4-176	AA		C	
VRS-RE3AAR39J	4-177	AB		C	
VRS-RE3LA151J	4-178	AC		C	
VRS-TQ2BB000J	6- 20	AA		C	
VRS-TQ2BB331J	10- 7	AA		C	
VRS-TQ2BB340J	10- 8	AB	N	C	
VRS-TQ2BB470J	10- 9	AB	N	C	
VRS-TS2AD000J	4- 43	AA		C	
"	4- 76	AA		C	
VRS-TS2AD100J	4- 77	AA		C	
VRS-TS2AD101J	4- 78	AA		C	
VRS-TS2AD102J	4- 79	AA		C	
"	6- 14	AA		C	
VRS-TS2AD103J	4- 81	AA		C	
"	6- 15	AA		C	
VRS-TS2AD104J	4- 82	AA		C	
"	8- 15	AA		C	
"	9- 10	AA		C	
VRS-TS2AD105J	4- 83	AA		C	
"	9- 11	AA		C	
VRS-TS2AD112J	4- 84	AA		C	
VRS-TS2AD122F	4- 85	AA		C	
VRS-TS2AD122J	4- 86	AA		C	
VRS-TS2AD123J	4- 87	AA		C	
VRS-TS2AD132G	4- 88	AA		C	
VRS-TS2AD133F	8- 8	AA		C	
VRS-TS2AD152G	4- 89	AA		C	
VRS-TS2AD152J	4- 90	AA		C	
VRS-TS2AD153J	4- 91	AA		C	
VRS-TS2AD162J	4- 92	AA		C	
VRS-TS2AD182G	4- 93	AA		C	
VRS-TS2AD183J	4- 94	AA		C	
VRS-TS2AD202J	9- 12	AA		C	
VRS-TS2AD203J	6- 16	AA		C	
VRS-TS2AD220J	4- 95	AA		C	
VRS-TS2AD222J	4- 96	AA		C	
"	8- 16	AA		C	
VRS-TS2AD223J	4- 97	AA		C	
VRS-TS2AD224J	8- 17	AA		C	
VRS-TS2AD272J	4- 98	AA		C	
VRS-TS2AD273G	9- 13	AC		C	
VRS-TS2AD273J	4- 99	AA		C	
VRS-TS2AD302J	4-100	AA		C	
VRS-TS2AD303F	4-101	AA		C	
VRS-TS2AD330J	4- 40	AA		C	
"	4-102	AA		C	
"	9- 14	AA		C	
VRS-TS2AD334J	4-103	AA		C	
VRS-TS2AD362F	4-104	AA		C	
VRS-TS2AD392G	4-105	AA		C	
VRS-TS2AD432J	4-106	AA		C	
VRS-TS2AD470J	4-107	AA		C	
VRS-TS2AD472G	4-109	AA		C	
VRS-TS2AD472J	4-108	AA		C	
"	8- 9	AA		C	
VRS-TS2AD473J	4-110	AA		C	
"	9- 15	AA		C	
VRS-TS2AD512F	4-111	AA		C	
VRS-TS2AD513J	4-112	AA		C	
VRS-TS2AD561J	4-113	AA		C	
VRS-TS2AD562J	4-114	AA		C	
VRS-TS2AD563J	4-115	AA		C	
VRS-TS2AD622J	4-116	AA		C	
VRS-TS2AD681J	4-117	AA		C	
VRS-TS2AD682J	4-118	AA		C	
VRS-TS2AD802J	4-119	AC	N	C	
VRS-TS2AD822J	6- 17	AA		C	

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