SHARP SERVICE MANUAL

CODE: 00ZERA610USME

ELECTRONIC CASH REGISTER

MODEL ER-A610

SRV Key : LKGIM7113RCZZ
PRINTER : M-820
(For "U" & "A" version)

CAUTION
EXTREME CAUTION MUST BE TAKEN WHEN SERVICING THIS MACHINE. EVEN THOUGH THE MODE SWITCH IS IN THE OFF POSITION, VOLTAGE IS STILL SUPPLIED TO THE ENTIRE MACHINE.
WHEN WORKING ON THIS MACHINE MAKE SURE THAT THE POWER CORD IS REMOVED FROM THE WALL OUTLET.

CONTENTS

Parts marked with "⚠" is important for maintaining the safety of the set. Be sure to replace these parts with specified ones for maintaining the safety and performance of the set.

SHARP CORPORATION

The RBRC™ Seal

The RBRC™ Seal on the easily removable nickel-cadmium battery pack contained in our product indicates that SHARP is voluntarily participating in an industry program to collect and recycle these battery packs at the end of their useful life, when taken out of service within the United States. The RBRC™ program provides a convenient alternative to placing spent nickel-cadmium battery packs into the trash or municipal waste stream, which is illegal in some areas.

SHARP's payments to RBRC™ makes it easy for you to drop off the spent battery pack at local retailers of replacement nickel-cadmium batteries, or at authorized SHARP product service centers. You may also contact your local recycling center for information on where to return the spent battery pack. SHARP's involvement in this program is part of its commitment to protecting our environment and conserving natural resources.

(RBRC™ is a trademark of the Rechargeable Battery Recycling Corporation.)

CHAPTER 1. SPECIFICATIONS

1. Appearance/Rating

1) Appearance

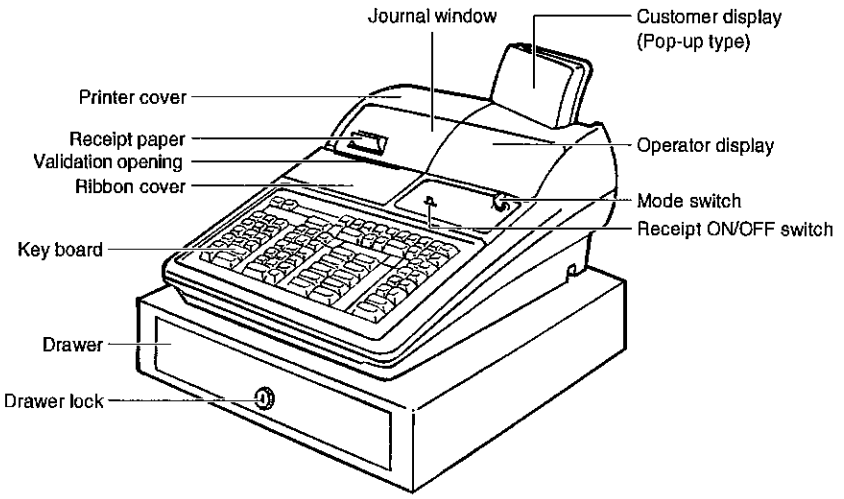


Fig. 1-1

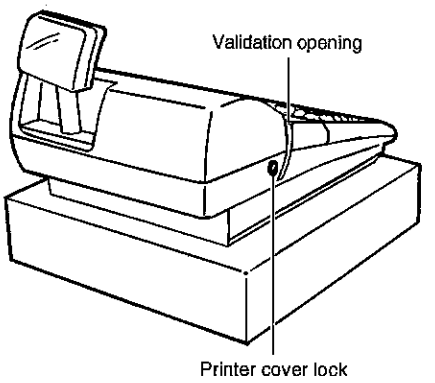


Fig. 1-2

2) Rating

Power source	AC local voltage (±10%) 60Hz
Power consumption	Standby: 20 W Maximum: 60 W with options installed.
Operating temperature	0°C~40°C (32°F~104°F)
Operating humidity	10%~90% (RH)
Physical dimensions, including the drawer	445(W) × 485(D) × 325(H)mm
Weight	17.8 kg

2. Keyboard

1) Standard keyboard layout

↑ RECEIPT	↑ JOUNAL					SERV #	PRICE 1	PRICE 2	PRICE 3	PRICE 4	PRICE 5	PRICE 6	CUS-TOMER	DELETE	NON-DELETE
				PLU/SUB			UPC		REPEAT	INQ	PRICE CHANGE		AMT	FS SHIFT	FS TEND
PRINT	#	SCALE		TAX	TAX1 SHIFT	TAX2 SHIFT								CH4	CH5
RCPT	⊖1	⊖2		@/ for	•	CL		5		10				CH2	CH3
CONV	%1	%2		7	8	9		4		9				CHK	CH1
NS	RA	PO		4	5	6		3		8				AUTO	MDSE SBTL
RFND	SBTL VOID			1	2	3		2		7				SBTL	
PAST VOID	DIRECT VOID			0		00		1		6				CA/AT	

Fig. 2-1

2) Key top name

① Standard key top

Keytop	Description
0 to 9, 00	Numeric keys
•	Decimal point key
C L	Clear key
@/FOR	Multiplication key
DEPT. 1~10	Department 1~10 keys
↑ RECEIPT	Receipt paper feed key
↑ JOURNAL	Journal paper feed key
RCPT	Receipt print key
PRINT	Validation print key
#	Non-add code entry key
AUTO	Atutomatically entry key
NS	No sale key
⊖ 1	Discount 1 key
⊖ 2	Discount 2 key
% 1	% 1 key
% 2	% 2 key
PO	Paid out key
RA	Received on account key
RFND	Refund key
AMT	Amount key
PLU/SUB	PLU/Subdept. code entry key
SBTL	Tax included subtotal key
CHK	Check key
CUSTOMER	Customer code entry key
UPC	UPC code entry key
REPEAT	Repeat key
INQ	UPC inquiry key
PRICE CHANGE	Price change key
DELETE	Delete key
NON DELETE	Non-delete key
SCALE	Scale entry key
PRICE 1~6	Price shift 1~6 keys
DIRECT VOID	Direct void key
PAST VOID	Past void key
SBTL VOID	Subtotal void key
TAX	Tax key
TAX 1 SHIFT	Tax 1 shift key
TAX 2 SHIFT	Tax 2 shift key
SERV#	Server number entry key
FS SHIFT	Food stamp shift key
FS TEND	Food stamp tender key
CONV	Currency conversion key
CH 1~5	Charge 1~5 keys
MDSE SBTL	Merchandise subtotal key
CA/AT	Cash & Amount tender key

② Option key top

Keytop	Description
DEPT. 11~99	Department 11~99 keys
PLU 1~126	Direct/Sub department 1~126 keys
⊖ 3, 4	Discount 3 and 4 keys
% 3, 4	%3 and 4 keys
CH6~8	Charge 6~8 keys
CA 2	Cash 2 key
AUTO 2 ~10	Automatically entry key 2~10
000	000 key
PO2	Paid out 2 key
DEPT#	Department nimber entry key
CONV 2~4	Currency conversion 2~4 keys
TAX 3 SHIFT	Tax 3 shift key
TAX 4 SHIFT	Tax 4 shift key
DEPOSIT	Deposit key
DEPOSIT RF	Deposit refund key

3. Mode switch

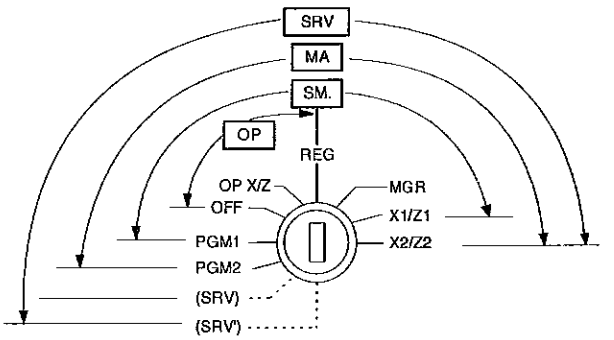


Fig. 3-1

* The key can be removed in the REG or OFF position.
* In the SRV' mode, key inputs are prohibited and no display is made.
* With the key in the off position power is still supplied to the main PWB.

[Functions]

- Function for each key position
- SRV': System reset
- SRV: Service mode (Service programming)
- PGM2: Allows programming of an item that is not changed frequently, in addition to the PGM1 mode programming.

- PGM1: Allows programming of items frequently changed (e.g. department, PLU pricing, and discount rate setting).
- OP/XZ: Allows X or Z operation by servers or cashiers.
- REG: Allows registrations.
- MGR: Allows the operations, by authorized person such as a manager (e.g. correction after transaction finished or cancellation of entry limits), which are not permitted to ordinary cashiers.
- X1/Z1: Allows reading and resetting of a day's sales total.
- X2/Z2: Allows reading or resetting sales totals in a specified period.
- OFF: Switching off the display to prevent key board entries.
  (The setting does not turn off the AC power.)

4. Display

1) Layout

① Operator display

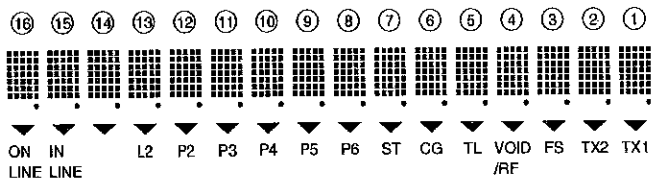


Fig. 4-1

	Dot display
No. of positions	16
Color of display	Green
Character size	8.15 (H) × 5.75 (W) mm
Font	Dot matrix (5×7)

② Customer display

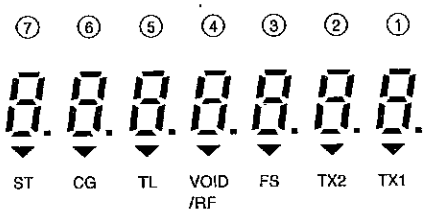


Fig. 4-2

No. of positions	7
Color of display	Green
Character size	13(H) × 6(W) mm
Font	7 segments

Lamps

Display contents	Description
ON LINE	The lamp lights up when the machine is connected to the online transmission line; and it goes off when the machine is disconnected from the line. The lamp blinks during data transmission.
IN LINE	The lamp lights up during inline communications.
ST	The lamp lights up when a subtotal is displayed.
TL	The lamp lights up when a transaction is finalized with CASH, CHECK, or CHARGE key, however, the lamp does not light up when a transaction is finalized with an amount tendered entry.
L2	Comes on when [L2] key is pressed.
CG	Comes on when change amount is displayed after tendering.
VOID/RFND	Comes on when [VOID] or [RFND] key is pressed or Refund type of sales is registered.
FS	Comes on when any item payable with food stamps is entered.
TX2	Comes on when [TAX 2 SHIFT] key is pressed or a taxable 2 item is entered.
TX1	Comes on when [TAX 1 SHIFT] key is pressed or a taxable 1 item is entered.
P2	Comes on when [P2] key is pressed.
P3	Comes on when [P3] key is pressed.
P4	Comes on when [P4] key is pressed.
P5	Comes on when [P5] key is pressed.
P6	Comes on when [P6] key is pressed.

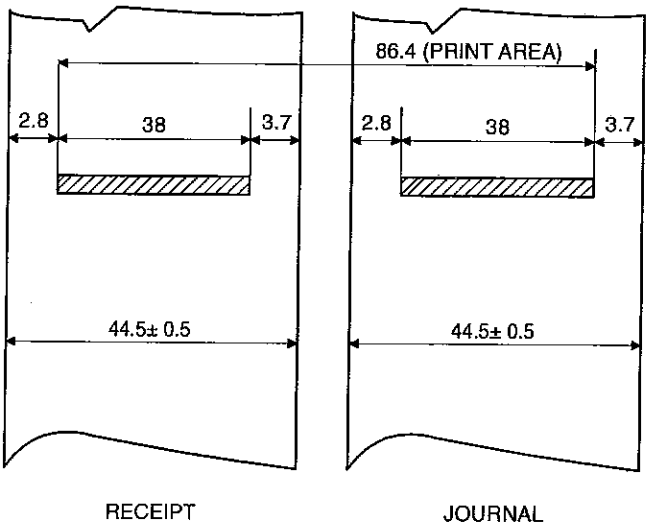
5. Printer (M-820)

1) Specifications

- Part number: M-820
- No. of stations: 2
- Printing system: Mechanical serial dot
- Direction of printing: Bidirectional
- Printing capacity: Receipt – 21 characters
  Journal – 21 characters
  Validation – 47 characters
  (one line only)
- Character size: 2.7 (H) × 1.5 (W) mm
  Print pitch:
  Column distance 1.83 mm
  Row distance 4.3 mm
- Total number of dots: (95 dots per line) × 2 (receipt and journal)
  Validation Max 213 dot
- Font: 7 × 7 dots
  Space between characters – 1 dot
- Distance between dots: 0.4 mm (H) × 0.407 mm (W)
- Journal near end sensor: Service route option
- Auto cutter: Set up (Full and partial cat.)
- Print speed: Approx. 2.5 lines/sec. (Approx. 26.4V)
- Paper feed speed: Receipt – Approx. 28.2 lines/sec.
  Journal – Approx. 11.2 lines/sec.
- Reliability: MCBF – 2 million lines (excluding the print head)
  Head life – 40 million characters (in the case of printing average 2 dots per character per wire
- Validation form sensor: Not setup

2) Printing area

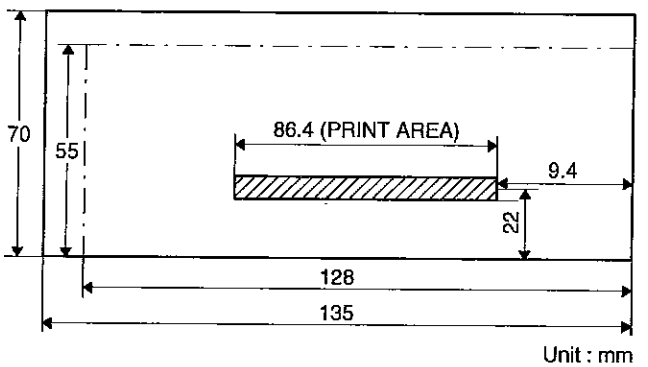
Receipt/journal



Unit : mm

Fig. 5-1

Validation form



Unit : mm

Fig. 5-2

3) Paper

- Paper roll dimensions: 44.5±0.5mm in width, 80mm in diameter
- Paper quality: Journal
  Bond paper (paper thickness: 0.06 to 0.09mm, paper weight: 52.3 to 64g/m^2)
  Validation form
  Thickness: 0.07 to 0.14mm
  Size: 135mm or more (W) × 70mm or more (H)

4) Inking

- Ink supply system: Ink ribbon
- Form: Cartridge
- Specification: Material – Nylon
- Ribbon life: 6 million characters
- Print color: Purple (single color)

5) Logo stamp

- Material: Porous rubber
- Stamp color: Purple (single color)
- Max. stamp size: 30(W) × 20(H) mm
- Ink refill: Allowed (UINK-1001CCZZ: 5CC)

CHAPTER 2. OPTIONS

1. System configuration

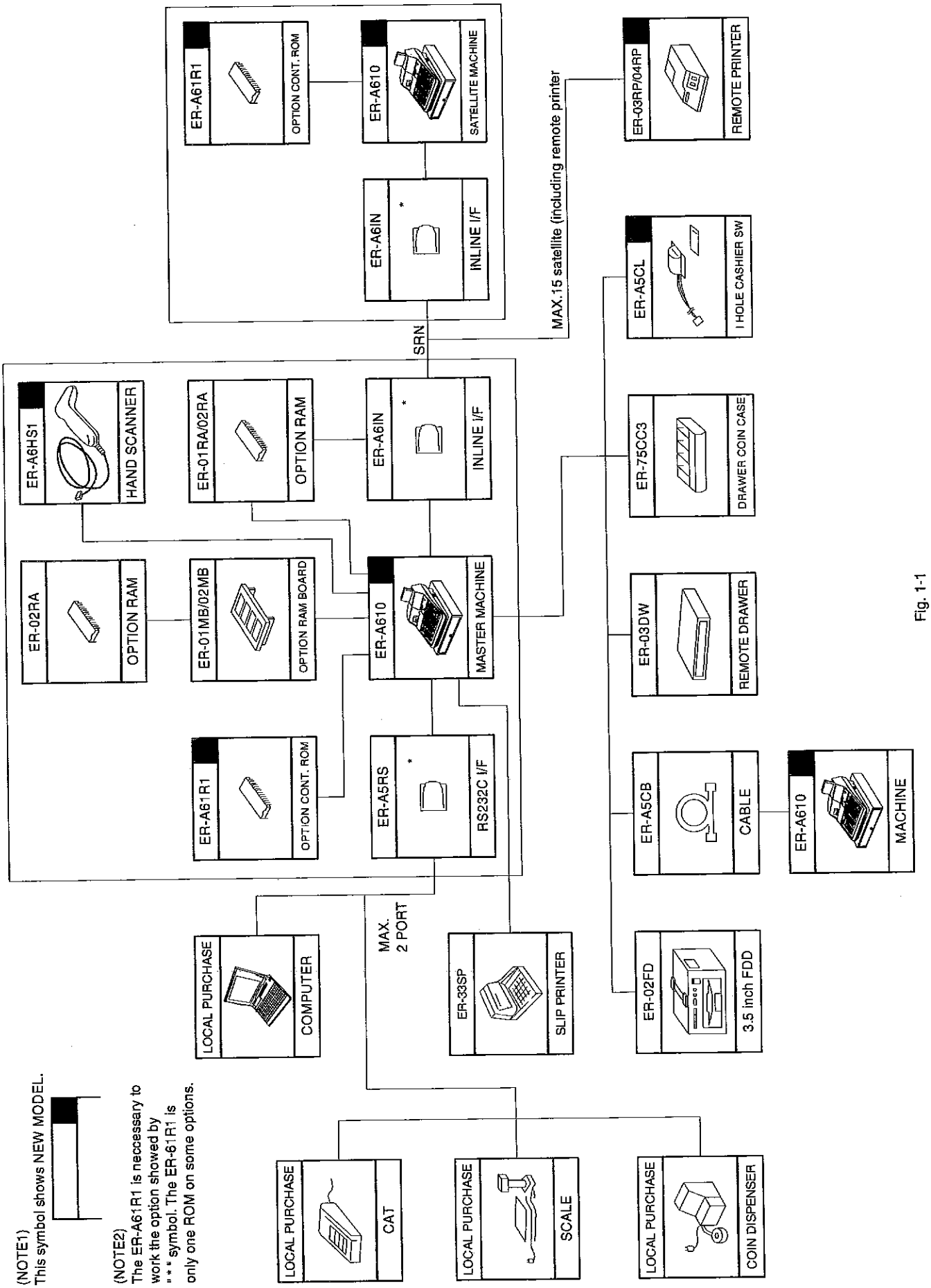


Fig. 1-1

2. Options

NO	NAME	MODEL	DESCRIPTION
1	REMOTE PRINTER	ER-03RP	Via SRN I/F (ER-A6IN)
		ER-04RP	
2	HAND SCANNER	ER-A6HS1	
3	REMOTE DRAWER	ER-03DW	7B/5C, MAX. 3 units
4	COIN CASE	ER-75CC3	7B/5C
5	1 HOLE CLERK KEY	ER-A5CL	
6	EXPANSION RAM CHIP	ER-01RA	32K bytes RAM chip
		ER-02RA	128K bytes RAM chip
7	EXPANSION MEMORY BOARD	ER-01MB	128K bytes memory board with 3 IC sockets (For ER-02RA)
		ER-02MB	1M bytes memory board
8	IN-LINE SYSTEM	ER-A6IN	SRN inline I/F
9	ON-LINE SYSTEM	ER-A5RS	2ports RS-232 I/F
10	CONTROL ROM	ER-A61R1	Control for ER-A6IN, ER-A5RS
11	PRESETS LOADER	ER-02FD	FD unit
12	CONNECTION CABLE	ER-A5CB	Loader cable
13	SLIP PRINTER	ER-33SP	
14	KEY TOP KIT	ER-11KT6	1 × 1 key top
		ER-12KT6	1 × 2 key top
		ER-22KT6	2 × 2 key top
		ER-11DK6	1 × 1 dummy key
		ER-51DK6	1 × 5 dummy key

3. Service options

NO.	NAME	PARTS CODE	PRICE RANK	DESCRIPTION
1	SERVICE KEY	LKGIM7113RCZZ	AK	For the mode switch
2	DRIP-PROOF SWITCH COVER	GCOVB7047RCZZ	BA	
3	MODE KEY GRIP COVER	LKGIM7126RCZZ	AL	OP key only
4	DRIP-PROOF KEYBOARD COVER	GCOVB7043RCZZ	BC	
5	JOURNAL NEAR END SENSOR	DKIT-8643RCZZ	BG	
6	PROGRAMMING CHARACTER KEYBOARD COVER	GCOVB7043RCSD	BG	
7	ADDITIONAL CLERK KEY (Option for ER-A5CL)	LKGIM7346RCZZ	AX	Key No. = 7
		LKGIM7347RCZZ	AX	Key No. = 8
		LKGIM7348RCZZ	AX	Key No. = 9
		LKGIM7349RCZZ	AX	Key No. = 10
		LKGIM7350RCZZ	AX	Key No. = 11
		LKGIM7351RCZZ	AX	Key No. = 12
		LKGIM7352RCZZ	AX	Key No. = 13
		LKGIM7353RCZZ	AX	Key No. = 14
		LKGIM7354RCZZ	AX	Key No. = 15

4. Service tools

NO.	NAME	PARTS CODE	PRICE RANK
1	EXPANSION PWB	CKOG-6708RCZZ	BU
2	SIO LOOP BACK CONECTOR	UKOG-6704RCZZ	AV
3	RS-232 LOOP BACK CONNECTOR	UKOG-6705RCZZ	BU

5. Supplies

NO.	NAME	PARTS CODE	PRICE RANK	DESCRIPTION
1	ROLL PAPER	DPAPR1006CSZZ	AR	5rolls/pack
2	INK RIBBON	PRBN-6640RCZZ	AX	
3	INK FOR STAMP	UINK-1001CCZZ	AK	5cc

6. Options

For installation of the options, refer to the Installation Manual which is separately issued from this manual.

7. How to use service tools

7-1. SIO loop back connector: UKOG-6704RCZZ

- External view

Signal	Pin
GND	1
$\overline{ER}$	2
$\overline{DR}$	3
RXD	4
TXD	5
$\overline{CD}$	6
$\overline{RR}$	7
$\overline{CS}$	8
$\overline{RS}$	9

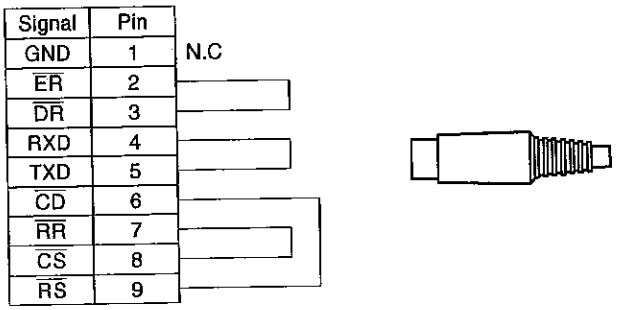


Fig. 7-1

- Purpose: Used for "SIO Test 1 (SIO loop back test)."
- Installation view:

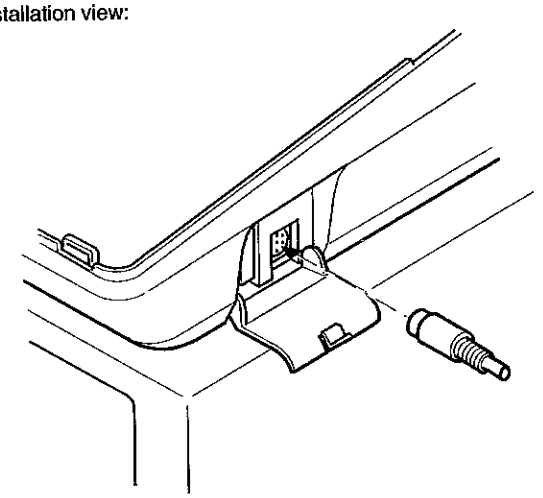


Fig. 7-2

- How to use: Connect the UKOG-6704RCZZ to the body and perform the following key operations:

  SRV mode: 117 → CA/AT

7-2. Expansion PWB: CKOG-6708RCZZ

- External view

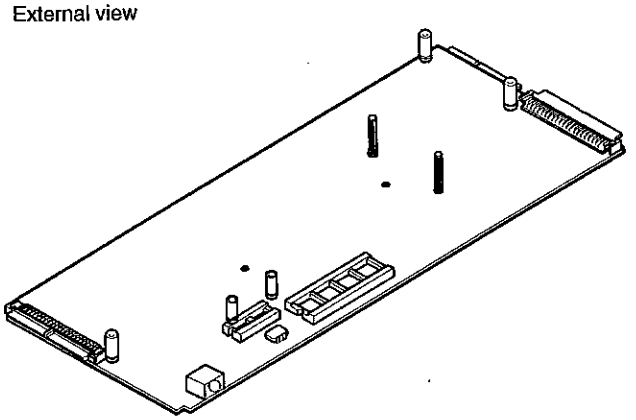


Fig. 7-3

Purpose 1: Used for servicing and repairing of options (such as the ER-A6IN and the ER-A5RS) which are connected with the main body option connector.

[Procedure 1]
Use an insulator base as that in Fig. 7-4 (shaded section) and perform servicing.

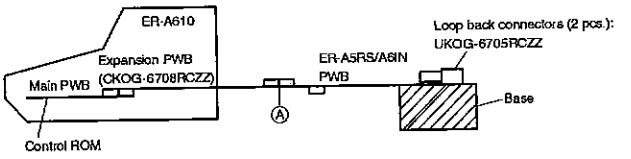


Fig. 7-4

To check the option I/F PWB from the solder side, connect the I/F PWB to OPTCN2. To check from the parts side, connect to OPTCN3.

(Note) The option I/F PWB should be held horizontally so that no excessive stress is applied to connecting section Ⓐ in Fig. 7-4.

[Procedure 2]

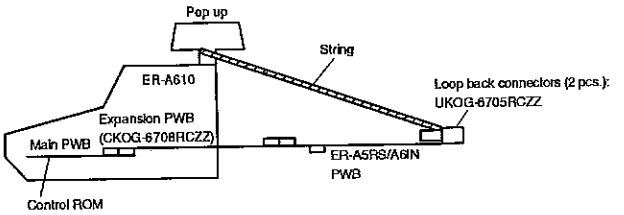


Fig. 7-5

As shown in Fig. 7-5, put a string between the pop up and the option PWB angle and adjust the length of the string so that the CKOG-6708RCZZ and the option PWB. Then perform servicing.

Purpose 2: The CKOG-6708RCZZ is equipped with the loop back connector for checking the ER-A5CB (SIO cable) cable operations.

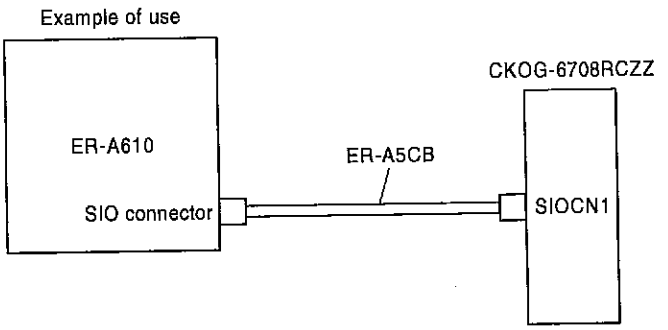


Fig. 7-6

Checking procedure

1) Connect the ER-A5CB between an ECR body and the CKOG-6708RCZZ SIOCN1. (The SIO functions of the ECR must be normal.)
2) Perform test function "117 (SIO loop back test)" and judge it normal or abnormal.

CHAPTER 3. SRV. RESET AND MASTER RESET

1. SRV. reset (Program Loop Reset)

Used to return the machine back to its operational state after a lock-up has occurred.

Procedure

- Method 1
  1) Turn off the AC switch.
  2) Set the mode switch to (SRV') position.
  3) Turn on the AC switch.
  4) Turn to (SRV) position from (SRV') position.
- Method 2
  1) Set the mode switch to PGM2 position.
  2) Turn off the AC switch.
  3) While holding down JOURNAL FEED key and RECEIPT FEED key, Turn on the AC switch.

Note: When disassembling and reassembling always power up using method 1 only. Method 2 will not reset the CKDC4.

Note: SRV programming job#926-B must be set to "4" to allow PGM program loop reset.

2. Master reset (All memory clear)

There are two possible methods to perform a master reset.

- MRS-1

Used to clear all memory contents and return machine back to its initial settings. return keyboard back to default. for default keyboard layout.

Procedure

1) Turn off the AC switch.
2) Set the MODE switch to the (SRV') position.
3) Turn on the AC switch.
4) While holding down JOURNAL FEED key, turn to (SRV) position from (SRV') position.

- MRS-2

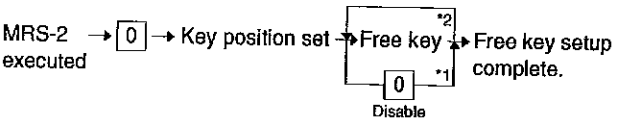
  Used to clear all memory and keyboard contents.
  This reset returns all programming back to defaults. The keyboard must be entered by hand.
  This reset is used if an application needs different keyboard layout other than that supplied by a normal MRS-1.

Procedure

1) Turn off the AC switch.
2) Set the MODE switch to the (SRV') position.
3) Turn on the AC switch.
4) While holding down JOURNAL FEED key and RECEIPT FEED key, turn to (SRV) position from (SRV') position.
5) Key position assignment:

* After the execution of MRS-2, only the RECEIPT FEED and JOURNAL FEED keys can remain effective on key assignment. Any key can be assigned on any key position on the main keyboard.

[key setup procedure]



NOTES:

*1: When the 0 key is pressed, the key of the key number on display is disabled.

*2: Push the key on the position to be assigned. With this, the key of the key number on display is assigned to that key position.

Key number	Key name	Key number	Key name
1	Numeric key "0"	9	Numeric key "8"
2	Numeric key "1"	10	Numeric key "9"
3	Numeric key "2"	11	Numeric key "00"
4	Numeric key "3"	13	Decimal point key
5	Numeric key "4"	14	CL key
6	Numeric key "5"	15	@/FOR key
7	Numeric key "6"	16	SBTL key
8	Numeric key "7"	17	CA/AT key

CHAPTER 4. HARD WARE DESCRIPTION

1. Hard ware block diagram

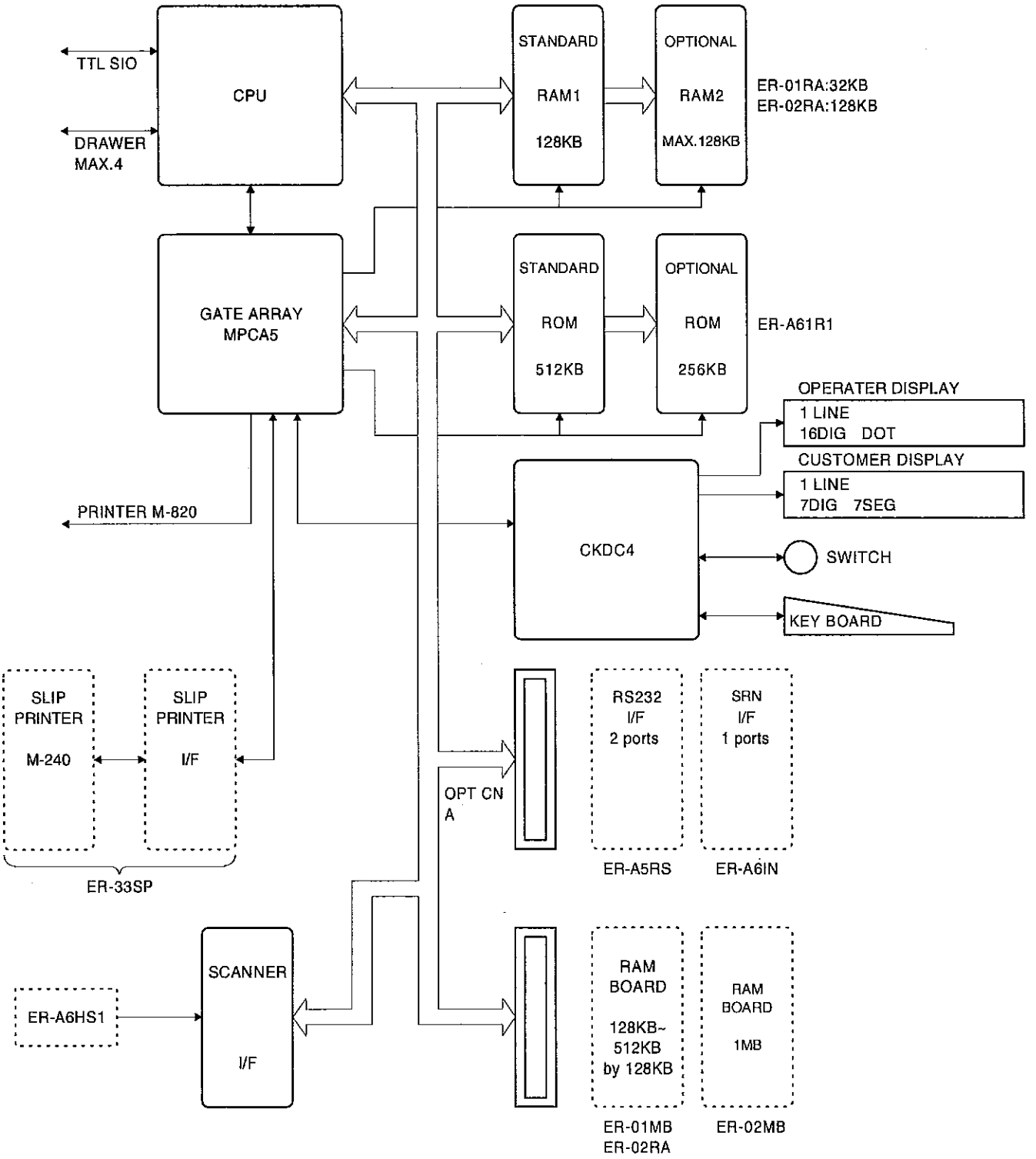
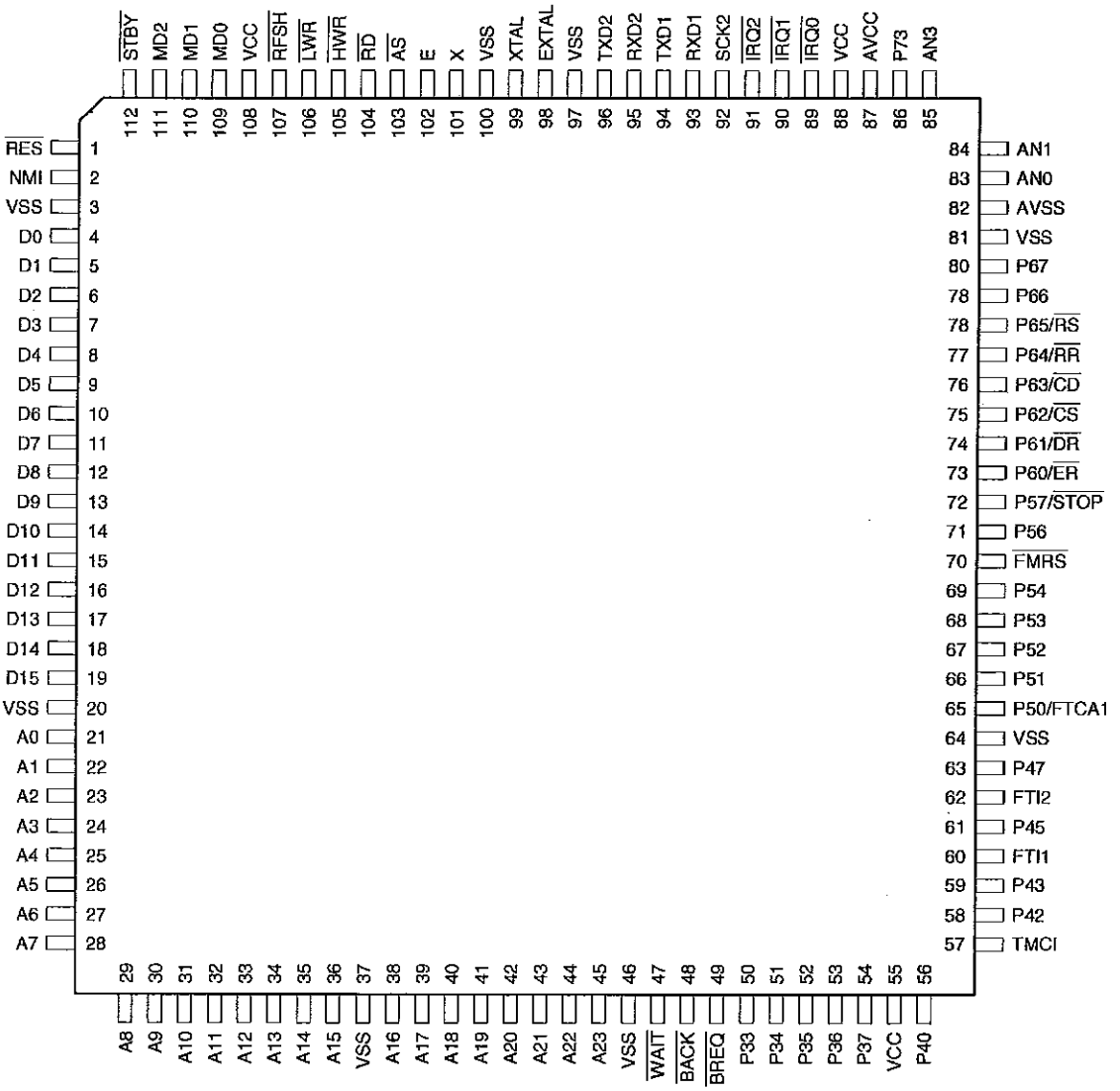


Fig. 1-1

2. Description of main LSI's

2-1. CPU (HD6415108FX)

1) Pin configuration



HD6415108FX pin configuration

Fig. 2-1

2) Block diagram

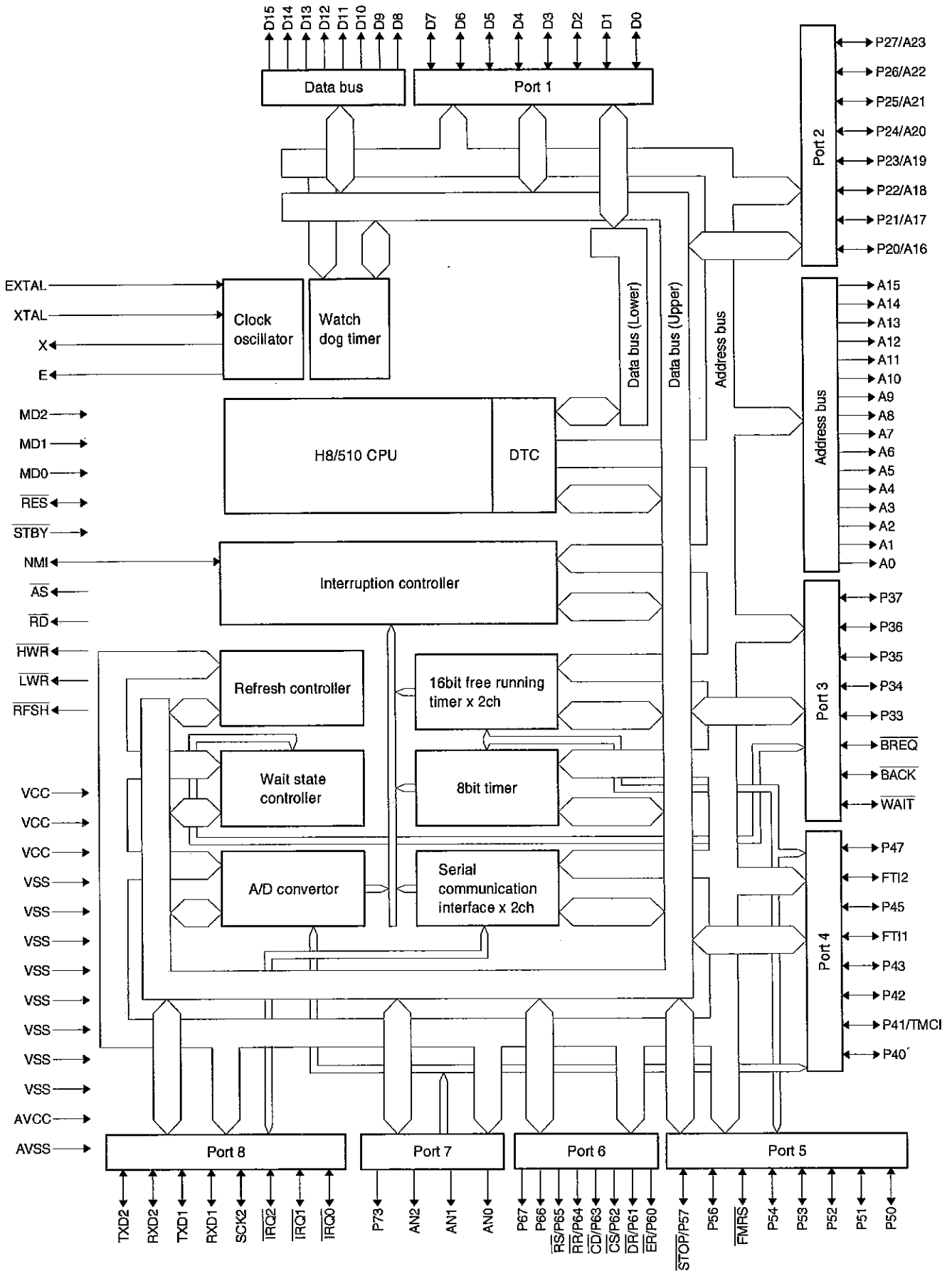


Fig. 2-2

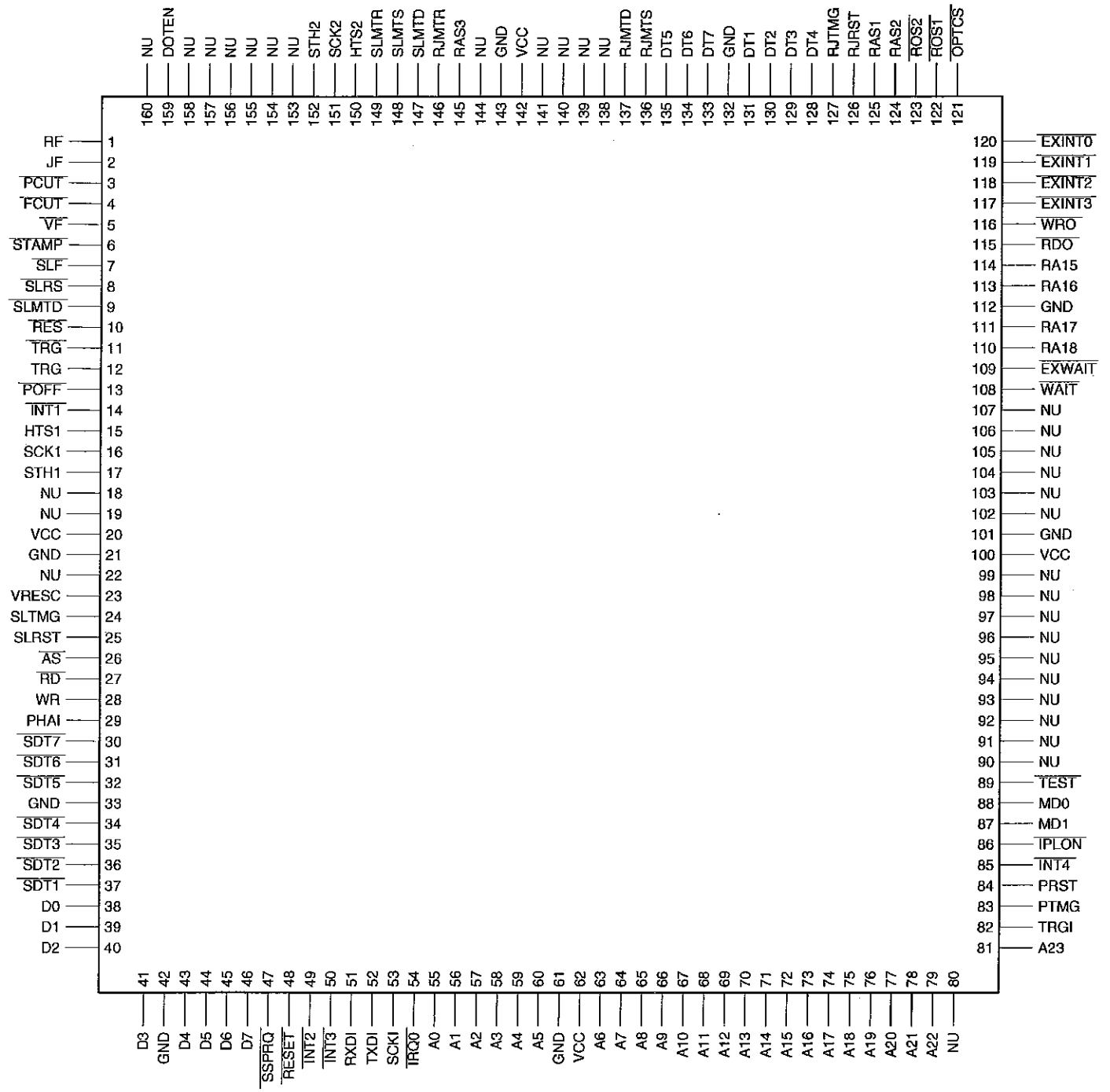
3) Pin description

Pin No.	Symbol	Signal name	In/ Out	Function
1	RES	RESET	I/O	Reset input
2	NMi	NMi	In	Non-maskable interrupt input for SSP interrupt input.
3	VSS	NU	In	GND
4	D0	Nu	In	GND
5	D1	Nu	In	GND
6	D2	Nu	In	GND
7	D3	Nu	In	GND
8	D4	Nu	In	GND
9	D5	Nu	In	GND
10	D6	Nu	In	GND
11	D7	Nu	In	GND
12	D8	D0	I/O	Data bus
13	D9	D1	I/O	Data bus
14	D10	D2	I/O	Data bus
15	D11	D3	I/O	Data bus
16	D12	D4	I/O	Data bus
17	D13	D5	I/O	Data bus
18	D14	D6	I/O	Data bus
19	D15	D7	I/O	Data bus
20	VSS	NU	In	GND
21	A0	A0	Out	Address bus
22	A1	A1	Out	Address bus
23	A2	A2	Out	Address bus
24	A3	A3	Out	Address bus
25	A4	A4	Out	Address bus
26	A5	A5	Out	Address bus
27	A6	A6	Out	Address bus
28	A7	A7	Out	Address bus
29	A8	A8	Out	Address bus
30	A9	A9	Out	Address bus
31	A10	A10	Out	Address bus
32	A11	A11	Out	Address bus
33	A12	A12	Out	Address bus
34	A13	A13	Out	Address bus
35	A14	A14	Out	Address bus
36	A15	A15	Out	Address bus
37	VSS	NU	In	GND
38	A16	A16	Out	Address bus
39	A17	A17	Out	Address bus
40	A18	A18	Out	Address bus
41	A19	A19	Out	Address bus
42	A20	A20	Out	Address bus
43	A21	A21	Out	Address bus
44	A22	A22	Out	Address bus
45	A23	A23	Out	Address bus
46	VSS	NU	In	GND
47	WAIT	WAIT	In	Wait signal
48	BACK	BACK	Out	Bus control request acknowledge
49	BREQ	BREQ	In	Bus control request
50	P33	DOPS	In	Drawer open signal
51	P34	DR0	Out	Option drawer open signal
52	P35	DR1	Out	Remote drawer No.1 open signal
53	P36	DR2	Out	Remote drawer No.2 open signal
54	P37	DR3	Out	Remote drawer No.3 open signal
55	VCC	VCC	In	+5V
56	P40	IFV	In	Slip printer (M-240) interface connect signal
57	TMCi	PTMG	In	Printer (M-820) timing signal
58	P42	TOF	In	Slip printer (M-240) TOF sensor signal
59	P43	BOF	In	Slip printer (M-240) BOF sensor signal
60	FTi1	PRST	In	Printer (M-820) reset signal
61	P45	NEJ	In	Near end sensor journal side
62	FTi2	SHEN	In	CKDC Interface shift enable signal
63	P47	NER	In	GND
64	VSS	VSS	In	GND
65	P50/FTCA1	TRGI	Out	Dot pulse adjust signal
66	P51	NU	Out	NC
67	P52	NU	Out	NC
68	P53	NU	In	GND
69	P54	NU	Out	NC
70	FMRS	NU	In	NC
71	P56	NU	Out	NC
72	P57/STOP	STOP	Out	System reset output. Normally
73	P60/ER	ERS/ER	Out	SIO control signal (Equipment ready)
74	P61/DR	DRS/DR	In	SIO control signal (Data set ready)
75	P62/CS	CSS/CS	In	SIO control signal (Clear to send)
76	P63/CD	CDS/CD	In	SIO control signal (Carrier detect)
77	P64/RR	RRS/RR	Out	SIO control signal (Ready to receive)
78	P65/RS	RSS/RS	Out	SIO control signal (Request to send)
79	P66	NU	In	GND
80	P67	NU	In	GND
81	VSS	NU	In	GND
82	AVSS	NU	In	GND
83	AN0	VPR	In	Validation sensor journal
84	AN1	VPJ	In	Validation sensor receipt
85	AN3	VPTEST	In	+24V test input
86	P73	VPPS	In	Validation sense signal
87	AVCC	AVCC	In	+5V
88	VCC	VCC	In	+5V
89	IRQ0	IRQ0	In	Interrupt signal 0
90	IRQ1	IRQ1	In	Interrupt signal 1
91	IRQ2	IRQ2	In	Interrupt signal 2
92	SCK2	SCKi	In	CKDC Interface sync shift clock
93	RXD1	RXD	In	SIO control signal (Receive data)
94	TXD1	TXD	Out	SIO control signal (Transmit data)

Pin No.	Symbol	Signal name	In/ Out	Function
95	RXD2	RXD2	In	CKDC Interface shift input data
96	TXD2	TXDi	Out	CKDC Interface shift output data
97	VSS	NU	In	GND
89	EXTAL	EXTAL	In	Crystal oscillator connection
99	XTAL	XTAL	In	Crystal oscillator connection
100	VSS	NU	In	GND
101	X	X	Out	System clock
102	E	NU	Out	Nu
103	$\overline{AS}$	$\overline{AS}$	Out	Address strobe
104	$\overline{RD}$	$\overline{RD}$	Out	Read
105	$\overline{HWR}$	$\overline{WR}$	Out	Write
106	$\overline{LWR}$	$\overline{LWR}$	Out	Nu
107	$\overline{RFSH}$	$\overline{RFSH}$	Out	Refresh cycle
108	VCC	VCC	In	+5V
109	MD0	MD0	In	+5V (MODE 3)
110	MD1	MD1	In	+5V (MODE 3)
111	MD2	MD2	In	GND
112	$\overline{STBY}$	$\overline{STBY}$	In	+5V (Nu)

2-2. G.A (MPCA5)

1) Pin configuration



GATE ARRAY (F258016PC)
MPCA5

Fig. 2-3

2) Block diagram

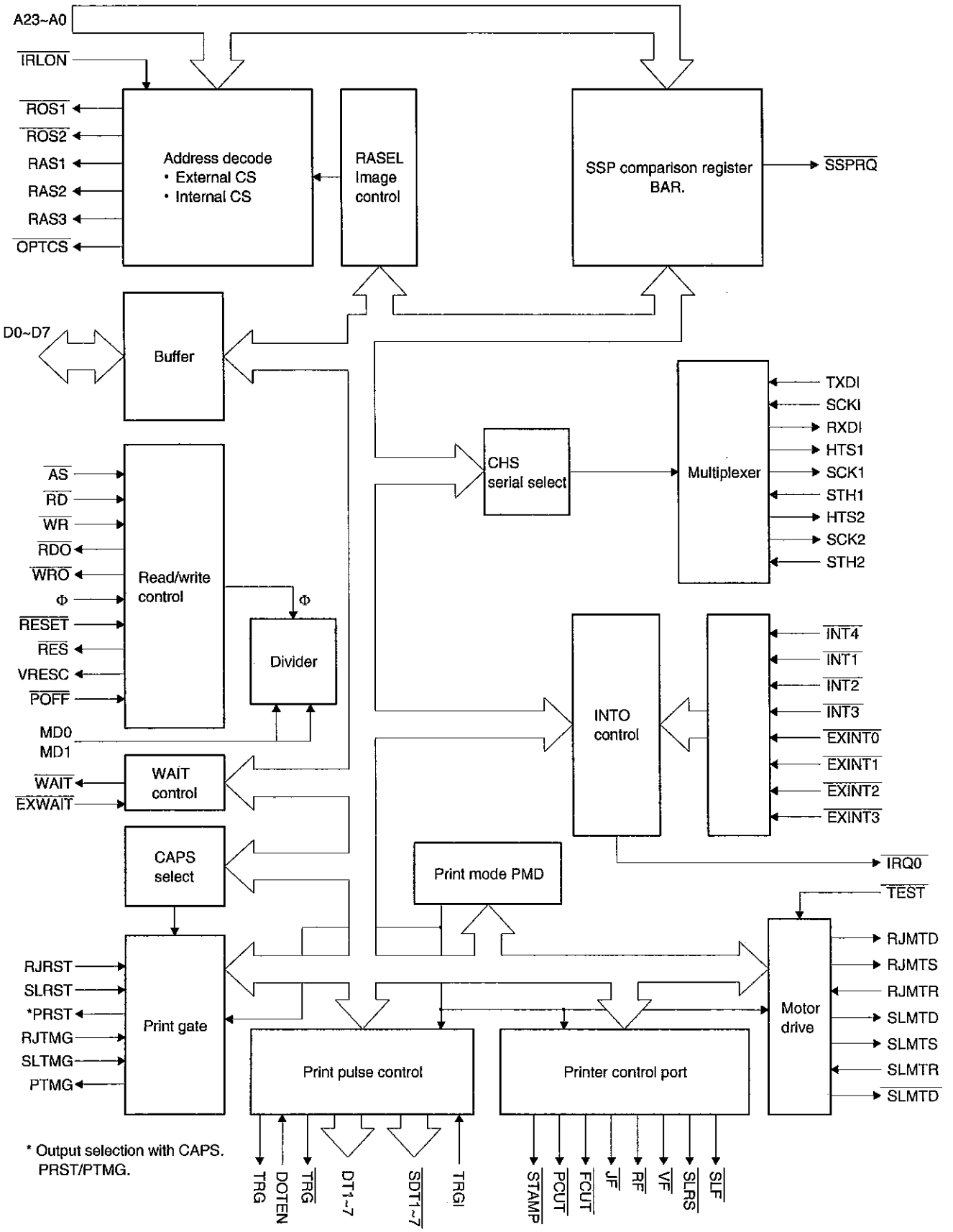


Fig. 2-4

3) Pin description

Pin No.	Signal name	In/ Out	Function
1	RF	Out	Receipt side paper feed solenoid
2	JF	Out	Journal side paper feed solenoid
3	$\overline{PCUT}$	Out	Printer (M-820) partial cut signal = Not used
4	$\overline{FCUT}$	Out	Printer (M-820) auto cut signal = Not used
5	$\overline{VF}$	Out	Multi line validation paper feed = Not used
6	$\overline{STAMP}$	Out	Printer (M-820) stamp signal
7	$\overline{SLFS}$	Out	Slip printer (M-240) paper feed singnal
8	$\overline{SLRS}$	Out	Slip printer (M-240) release signal
9	$\overline{SLMTD}$	Out	Slip printer (M-240) motor drive signal
10	$\overline{RES}$	Out	Peripheral output reset
11	$\overline{TRG}$	Out	Dot head trigger signal (M-240)
12	TRG	Out	Dot head trigger signal (M-820)
13	$\overline{POFF}$	In	Interrupt input
14	$\overline{INT1}$	In	Interrupt signal (Key interrupt request)
15	HTS1	Out	8 bit serial port output
16	SCK1	Out	Serial port shift clock output
17	STH1	In	8 bit serial port input
18	—	—	Nu
19	—	—	Nu
20	VCC	—	+5V
21	GND	—	GND
22	—	—	Nu
23	VRESC	Out	Turns active when reset and power down is met
24	SLTMG	In	Slip printer timing signal
25	SLRST	In	Slip printer reset signal
26	$\overline{AS}$	In	Address strobe
27	$\overline{RD}$	In	Read strobe
28	$\overline{WR}$	In	Write strobe
29	ϕ	In	(ϕ) System clock
30	$\overline{SDT7}$	Out	Printhead drive signal (dot7)
31	$\overline{SDT6}$	Out	Printhead drive signal (dot6)
32	$\overline{SDT5}$	Out	Printhead drive signal (dot5)
33	GND	—	GND
34	$\overline{SDT4}$	Out	Printhead drive signal (dot4)
35	$\overline{SDT3}$	Out	Printhead drive signal (dot3)
36	$\overline{SDT2}$	Out	Printhead drive signal (dot2)
37	$\overline{SDT1}$	Out	Printhead drive signal (dot1)
38	D0	I/O	Data bus
39	D1	I/O	Data bus
40	D2	I/O	Data bus
41	D3	I/O	Data bus
42	GND	—	GND
43	D4	I/0	Data bus
44	D5	I/0	Data bus
45	D6	I/0	Data bus
46	D7	I/0	Data bus
47	$\overline{SPRQ}$	Out	SSP interrupt request
48	$\overline{RESET}$	In	MPCA5 reset
49	$\overline{INT2}$	In	Interrupt signal (Nu)
50	$\overline{INT3}$	In	Interrupt signal (Nu)
51	RXDI	Out	8 bit serial port output to CPU
52	TXDI	In	8 bit serial port input from CPU

Pin No.	Signal name	In/ Out	Function
53	SCKI	In	Serial port shift clock input from CPU.
54	$\overline{IRQ0}$	Out	Interrupt request to CPU
55	A0	In	Address bus
56	A1	In	Address bus
57	A2	In	Address bus
58	A3	In	Address bus
59	A4	In	Address bus
60	A5	In	Address bus
61	GND	—	GND
62	VCC	—	+5V
63	A6	In	Address bus
64	A7	In	Address bus
65	A8	In	Address bus
66	A9	In	Address bus
67	A10	In	Address bus
68	A11	In	Address bus
69	A12	In	Address bus
70	A13	In	Address bus
71	A14	In	Address bus
72	A15	In	Address bus
73	A16	In	Address bus
74	A17	In	Address bus
75	A18	In	Address bus
76	A19	In	Address bus
77	A20	In	Address bus
78	A21	In	Address bus
79	A22	In	Address bus
80	—	—	Nu
81	A23	In	Address bus
82	TRGI	In	Dot pulse control/drive signal
83	$\overline{PTMG}$	Out	Printer timing signal
84	$\overline{PRST}$	Out	Printer reset signal
85	$\overline{INT4}$	In	Interrupt signal
86	$\overline{IPLON}$	In	Nu
87	MD1	In	Mode select input
88	MD0	In	Mode select input
89	$\overline{TEST}$	In	Nu
90	—	—	Nu
91	—	—	Nu
92	—	—	Nu
93	—	—	Nu
94	—	—	Nu
95	—	—	Nu
96	—	—	Nu
97	—	—	Nu
98	—	—	Nu
99	—	—	Nu
100	VCC	—	+5V
101	GND	—	GND
102	—	—	Nu
103	—	—	Nu
104	—	—	Nu
105	—	—	Nu
106	—	—	Nu

Pin No.	Signal name	In/ Out	Function	
107	—	—	Nu	
108	$\overline{WAIT}$	Out	Wait request signal	
109	$\overline{EXWAIT}$	In	External wait control input signal	
110	RA18	Out	Nu	
111	RA17	Out	Nu	
112	GND	—	GND	
113	RA16	Out	Nu	
114	RA15	Out	Nu	
115	$\overline{RDO}$	Out	Expansion RD signal	Option
116	$\overline{WRO}$	Out	Expansion WR signal	
117	$\overline{EXINT3}$	In	Expansion interruption signal 3	Option
118	$\overline{EXINT2}$	In	Expansion interruption signal 2	
119	$\overline{EXINT1}$	In	Expansion interruption signal 1	
120	$\overline{EXINT0}$	In	Expansion interruption signal 0	
121	$\overline{OPTCS}$	Out	Chip select base signal for expansion option	
122	$\overline{ROS1}$	Out	ROM 1 chip select signal	
123	$\overline{ROS2}$	Out	ROM 2 chip select signal	
124	RAS2	Out	RAM 2 chip select signal	
125	RAS1	Out	RAM 1 ship select signal	
126	RJRST	In	M820 reset signal	
127	RJTMG	In	M820 timing signal	
128	DT4	Out	M820 dot signal	
129	DT3	Out	M820 dot signal	
130	DT2	Out	M820 dot signal	
131	DT1	Out	M820 dot signal	
132	GND	—	GND	
133	DT7	Out	M820 dot signal	
134	DT6	Out	M820 dot signal	
135	DT5	Out	M820 dot signal	
136	RJMTS	Out	M820 motor brake signal	
137	RJMTD	Out	M820 motor drive signal	
138	—	—	Nu	
139	—	—	Nu	
140	—	—	Nu	
141	—	—	Nu	
142	VCC	—	+5V	
143	GND	—	GND	
144	—	—	Nu	
145	RAS3	Out	Nu	
146	RJMTR	In	M820 motor lock detection signal	
147	SLMTD	In	Nu	
148	SLMTS	In	Nu	
149	SLMTR	In	GND	
150	HTS2	Out	Nu	
151	SCK2	Out	Nu	
152	STH2	In	Nu	
153	—	—	Nu	
154	—	—	Nu	
155	—	—	Nu	
156	—	—	Nu	
157	—	—	Nu	
158	—	—	Nu	
159	DOTEN	Out	Dot drive enable signal	
160	—	—	Nu	

2-3. CKDC4 (HD404728A20FS)

1) General description

The CKDC4 is a 4-bit microcomputer developed for the ER-A670 and provides functions to control the real-time clock, keys, and displays. The basic functions of the CKDC4 are shown below.

Keys: The CKDC4 is capable of controlling a maximum of 256 momentary keys. (Sharp 2-key rollover control)
Simultaneous scanning of key and switch
(When a key is scanned, the state of a mode and clerk switch is also buffered. The host can scan the state of switch together with the key entry data at the same time the key is scanned.)

Switches: Mode switch with 14 positions maximum
8-bit clerk (cashier) switch
2-bit feed switch
1-bit receipt on/off switch
1-bit option switch
4-bit general-purpose switch (1-bit is used for keyboard select)

Displays: 16-column dot display
12-column 7-segment display (column digit selectable)
All column blink controlled for the dot and 7-segment display decimal point and indicators
Programmable patterns for 7-segment display:
Four patterns
Internal driver for 7-segment display

Buzzer: Single tone control

Clock: Year, month, day of month, day of week, hour, minute

Alarm: Hour, minute

Interrupt request (event control):
Detection of key input, switch position change, alarm issue, and counter overflow

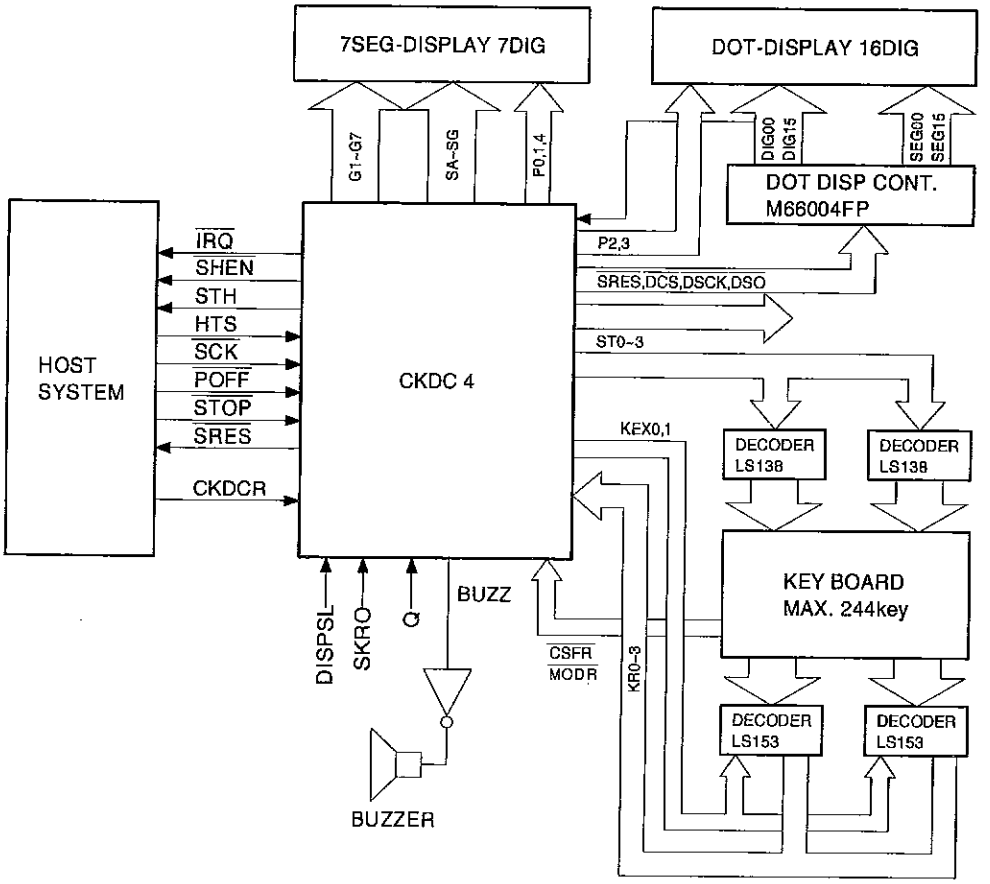


Fig. 2-5

2) Pin assignment

Pin No.	Port	I/O	RESET State	Signal name	I/O	Notes	PULL-UP -DOWN
1	$R0_1$	I/O	H-Z	SB	O	DB4 : SEG-B	PULL-DOWN
2	$R0_2$	I/O	H-Z	SC	O	DB4 : SEG-C	PULL-DOWN
3	$R0_3$	I/O	H-Z	SD	O	DB4 : SEG-D	PULL-DOWN
4	$R1_0$	I/O	H-Z	SE	O	DB4 : SEG-E	PULL-DOWN
5	$R1_1$	I/O	H-Z	SF	O	DB4 : SEG-F	PULL-DOWN
6	$R1_2$	I/O	H-Z	SG	O	DB4 : SEG-G	PULL-DOWN
7	$R1_3$	I/O	H-Z	AP	O	DB7 : 7SEG COM	PULL-DOWN
8	$R2_0$	I/O	H-Z	DDP	O	DB2 : DOT DP	PULL-DOWN
9	$R2_1$	I/O	H-Z	DID	O	DB3 : DOT COM	PULL-DOWN
10	$R2_2$	I/O	H-Z	DP	O	DB5 : 7SEG DP	PULL-DOWN
11	$R2_3$	I/O	H-Z	ID	O	DB5 : 7SEG ID	PULL-DOWN
12	RA_0	I	I	$\overline{MODR}$	I	MODE RETURN	PULL-UP
13	RA_1	I	I	$\overline{CFSR}$	I	CLEARK, FEED, SWITCH RETURN	PULL-UP
14	$R3_0$	I/O	H-Z	KEX0	O	KEY EXCHANGE0	
15	$R3_1$	I/O	H-Z	KEX1	O	KEY EXCHANGE1	
16	$R3_2$	I/O	H-Z	NU	O	GND	
17	$R3_3$	I/O	H-Z	NU	O	GND	
18	$R5_0$	I/O	I	ST0	O	KEY SCAN ST0	
19	$R5_1$	I/O	I	ST1	O	KEY SCAN ST1	
20	$R5_2$	I/O	I	ST2	O	KEY SCAN ST2	
21	$R5_3$	I/O	I	ST3	O	KEY SCAN ST3	
22	$R6_0$/INT0	I/O	I	$\overline{POFF}$	I	P-OFF	
23	$R6_1$/INT1	I/O	I	$\overline{STOP}$	I	STOP	PULL-UP
24	$R6_2$/INT2	I/O	I	$\overline{DDIG}$	O	DOT DISPLAY DIGIT INPUT	
25	$R6_3$/INT3	I/O	I	$\overline{DCS}$	O	DOT DISPLAY CONT./CS	
26	Vcc					Power supply	
27	$R4_0$/SCK	I/O	I	$\overline{SCK}$	I	SCK	
28	$R4_1$/SI	I/O	I	HTS	I	HTS	
29	$R4_2$/SO	I/O	I	STH	O	STH	
30	$R4_3$/PWM	I/O	I	SDISP	I	DIST SELECT	
31	$R7_0$/BUZZ	I/O	I	BUZZ	O	BUZZER	
32	$R7_1$/SCK2	I/O	I	$\overline{DSCK}$	O	DOT DISP CONT. SCK	
33	$R7_2$/SI2	I/O	I	$\overline{SRES}$	O	SYSTEM RESET	PULL-DOWN
34	$R7_3$/SO2	I/O	O	DSO	O	DOT DISP CONT. SO	
35	$R8_0$	I/O	O	$\overline{SHEN}$	O	$\overline{SHEN}$	
36	$R8_1$	I/O	O	$\overline{KRQ}$	O	KEY REQUEST	
37	$R9_0$	I	I	KR0	I	KEY RETURN 0	
38	$R9_1$	I	I	KR1	I	KEY RETURN 1	
39	$R9_2$	I	I	KR2	I	KEY RETURN 2	
40	$R9_3$	I	I	KR3	I	KEY RETURN 3	
41	RESET	I	I	CKDCR	I	CKDC IV RESET	
42	OSC2					4.19 MHz X'tal	
43	OSC1						
44	GND					GND	
45	CL1					32.768 KHz OSC	
46	CL2						
47	TEST	I	I	VCKDC		5V	
48	D0	I/O	H-Z	G1	O	7 SEG DIG 1	PULL-DOWN
49	D1	I/O	H-Z	G2	O	7 SEG DIG 2	PULL-DOWN
50	D2	I/O	H-Z	G3	O	7 SEG DIG 3	PULL-DOWN
51	D3	I/O	H-Z	G4	I	7 SEG DIG 4	PULL-DOWN
52	D4	I/O	H-Z	G5	O	7 SEG DIG 5	PULL-DOWN
53	D5	I/O	H-Z	G6	O	7 SEG DIG 6	PULL-DOWN
54	D6	I/O	H-Z	G7	O	7 SEG DIG 7	PULL-DOWN
55	D7	I/O	H-Z	NU	O		PULL-DOWN
56	D8	I/O	H-Z	NU	O		PULL-DOWN
57	D9	I/O	H-Z	NU	O		PULL-DOWN
58	D10	I/O	H-Z	NU	O		PULL-DOWN
59	D11	I/O	H-Z	NU	O		
60	D12	I/O	H-Z	NU	O		
61	D13	I/O	H-Z	NU	O		
62	D14	I/O	H-Z	NU	O		
63	D15	I/O	H-Z	NU	O		
64	$R0_0$	I/O	H-Z	SA	O	DB4 : SEG-A	PULL-DOWN

NOTE 3: Pull-up/down in the table indicates that the lines concerned require external pull-up/down resistance.

3. Clock generator

1) CPU (HD6415108FX)

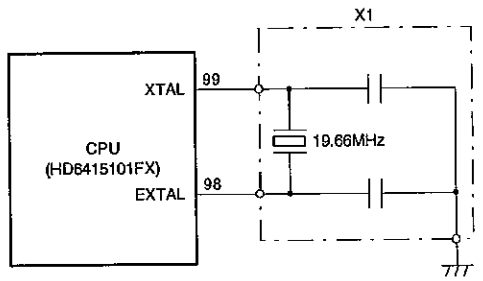


Fig. 3-1

Basic clock is supplied from a 19.66MHz ceramic oscillator.
The CPU contains an oscillation circuit from which the basic clock is internally driven. If the CPU was not operating properly, the signal does not appear on this line in most cases.

2) HD404728A20FS CKDC-III oscillation circuit (Display-PWB)

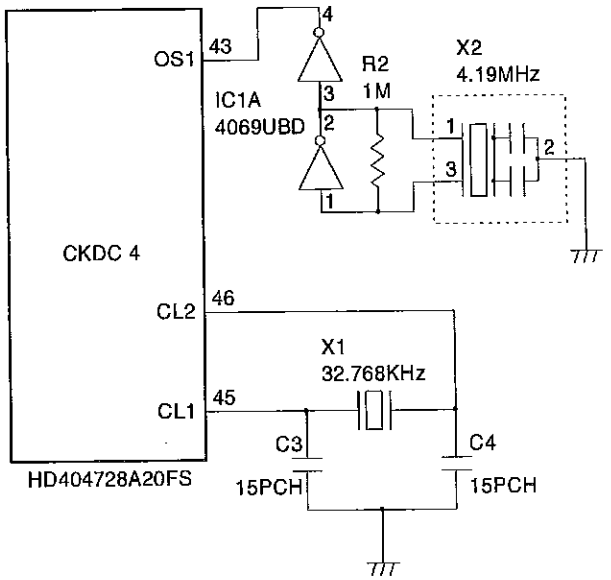


Fig. 3-2

Two oscillators are connected to the CKDC4.
The main clock X2 generates 4.19MHz which is used during power on.
When power is turned off, the CKDC4 goes into the standby mode and the main clock stops.
The sub-clock X1 generates 32.768KHz which is primarily used to update the internal RTC (real time clock). During the standby mode, it keeps oscillating to update the clock and monitoring the power recovery.

4. Reset (POFF) circuit

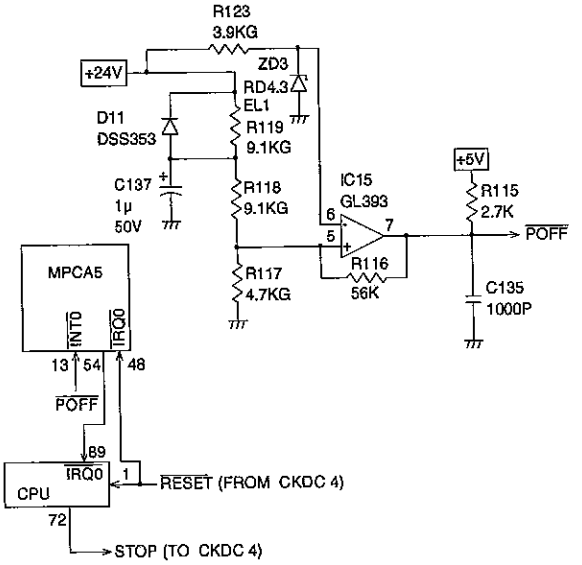


Fig. 4-1

In order to prevent memory loss at a time of power off and power supply failure of the ECR, the power supply condition is monitored at all times. When a power failure is met, the CPU suspends the execution of the current program and immediately executes the power-off program to save the data in the CPU registers in the external S-RAM with the signal $\overline{\text{STOP}}$ forced low to prepare for the power-off situation. The signal $\overline{\text{STOP}}$ is supplied to the CKDC4 as signal $\overline{\text{RESET}}$ to reset the devices.
This circuit monitors +24V supply voltage.
The voltage at the (–) pin of the comparator GL393 is always maintained to 4.3V by means of the zener diode ZD3, while +24V supply voltage is divided through the resistors R119, R118, and R117, and is applied to the (+) pin. When normal +24V is in supply, 5.1V is supplied to the (+) pin, therefore, signal $\overline{\text{POFF}}$ is at a high level. When +24V supply voltage decreases due to a power off or any other reason, the voltage at the (+) pin also decreases. When +24V supply voltage drops, the voltage at the (+) pin drops below +4.3V, which causes $\overline{\text{POFF}}$ to go low, thus predicting the power-off situation.

5. Memory control

1) Memory map

① **All range memory map**

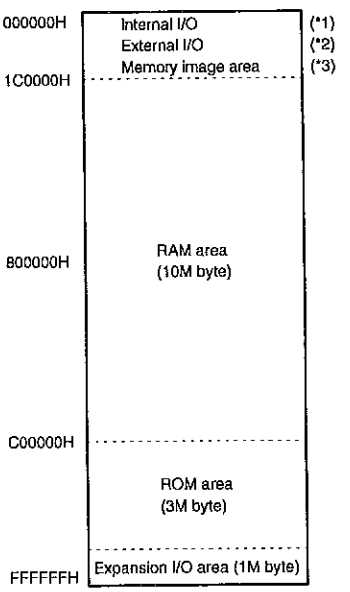


Fig. 5-1

(*1) "Internal I/O" means the registers in the H8/510.

(*2) "External I/O" means the base system I/O area to be addressed in page 0.

(*3) "Memory image area" means the lower 32KB of ROM area which is projected to 000000H ~ 007FFFH for allowing reset start and other vector addressing, or the lower 32KB of ROM area which is projected to 008000H ~ 00FE7FH for allowing 0 page addressing of work RAM area.

(*4) "Expansion I/O" means expansion I/O device area which isaddressed to area other than page 0.

② 0 page memory map

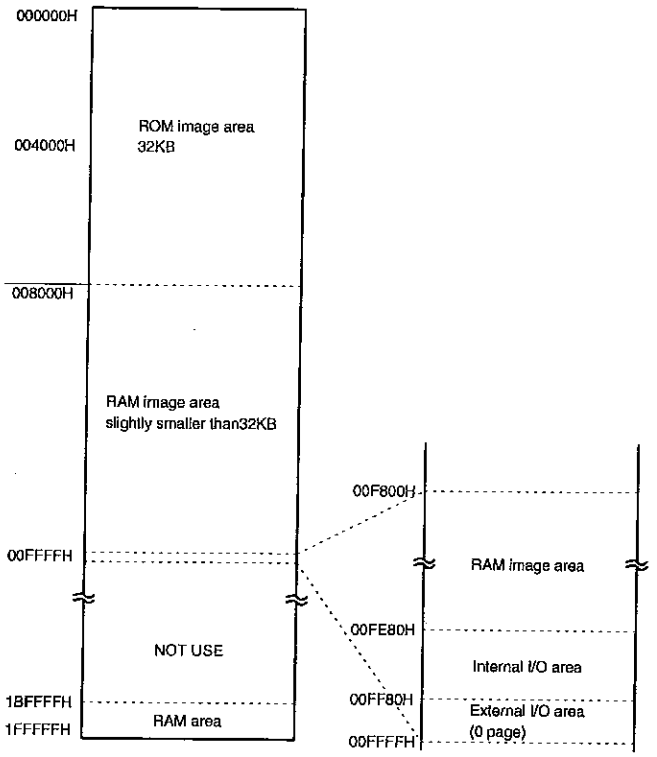


Fig. 5-2

- ROM image area: Image is formed in ROM area address C00000H C07FFFH. This area is identical to IPL ROM area which will beseparately developed.
- RAM image area: Image is formed in RAM area address 1D8000H1DFE7FH. (*Note)

  * Note: Image can be formed in lower 32KB of RAS2.

③ ROM area memory map

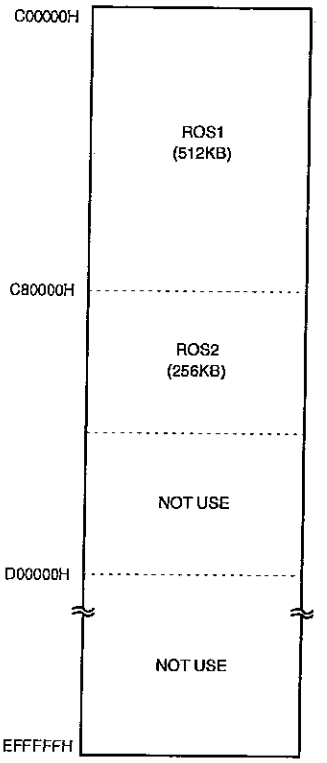


Fig. 5-3

These two decode signals decode 512KB space respectively and canbe used with max. 4MB ROM.

* Note: The lower 32KB of ROS1 signal is formed as OR of image area in 0page.

④ RAM area memory map

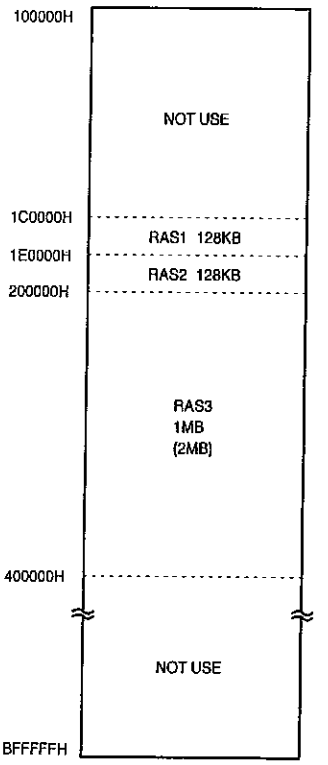


Fig. 5-4

In the three RAM chip select, the following address is decoded.

CS signal	Address
• RAS1	1C0000H~1DFFFFH (008000H~00FE7FH) ∗ Note
• RAS2	1E0000H~1FFFFFH (008000H~00FE7FH) ∗ Note
• RAS3	200000H~3FFFFFH

∗ Base signal is for 2M.

∗ Note: RAS1 signal is formed as OR in the image area of 0 page.j (Lower 32KB).
RAS2 signal is formed as OR in the image area of 0 page. (lower32KB).

⑤ I/O area memory map

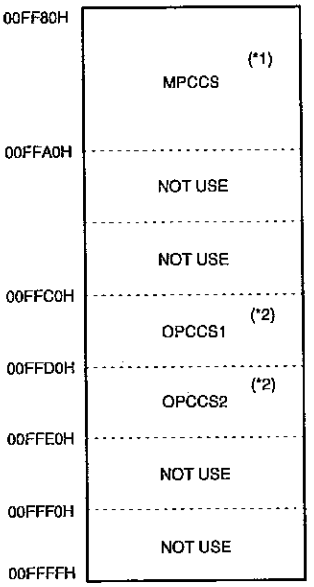


Fig. 5-5

∗ Note 1: MPCCS signal is the base signal for MPCA5 internal registerdecoding, and does not exist as an internal signal.

∗ Note 2: OPCCS1 and OPCCS2 signals are decoded in the OPC (optionperipheral controller) using the base signal OPTCS for optiondecoding. They does not exist as external signals.

2) Block diagram

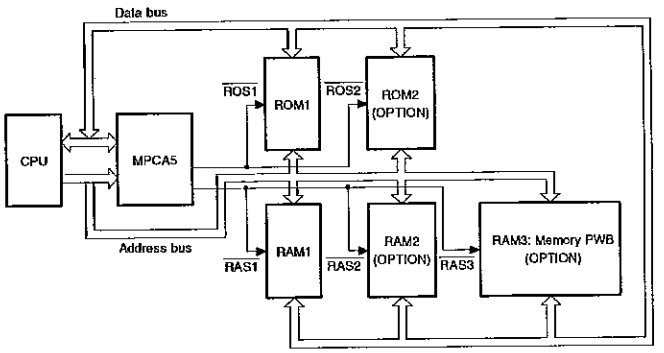


Fig. 5-6

① ROM control

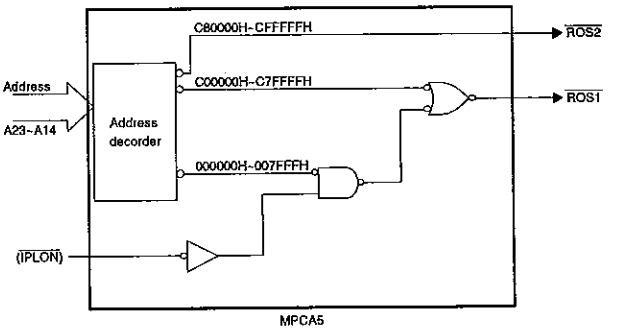


Fig. 5-7

IPLON: IPL board detection signal incorporated in the option slot. Note used in the ER-A650. (Not used)

Access is performed with two ROM chip select signals $\overline{ROS1}$ and $\overline{ROS2}$, which decode 512KB address area respectively to accessmax. 4MB ROM.

② RAM control

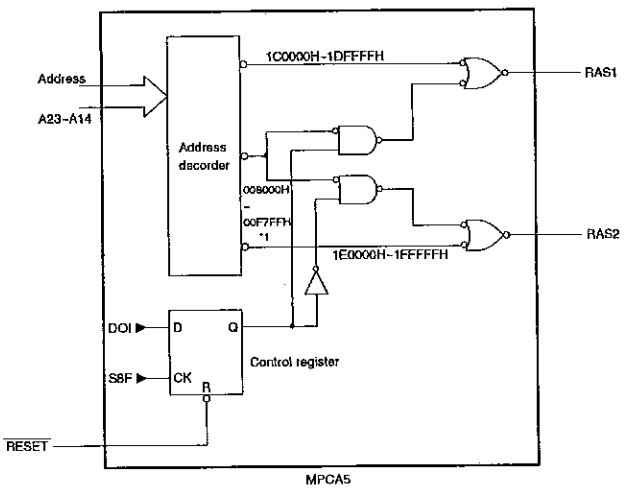


Fig. 5-8

Access is performed with two RAM chip select signals RAS1, RAS2 and RAS3. The control register in MPCA5 allows selection of pageimage memory area. (RAS1 is selected for initializing.)

∗ : For 0 page image area, selection between RAS1 and RAS2 can bemade with the control register. The 0 page control registerperforms initializing at the timing of no stack processimmediately after resetting.

6. SSP circuit

1) Block diagram

This is the circuit employed to do the Special Service Preset(SSP).

(Block diagram)

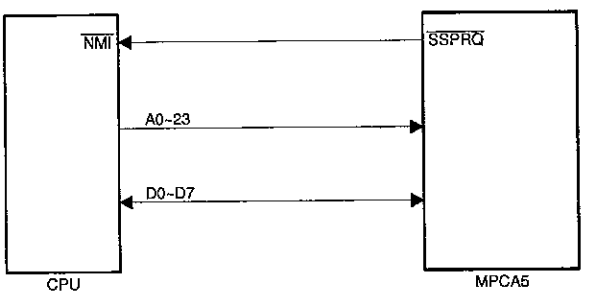


Fig. 6-1

(MPCA5 block diagram)

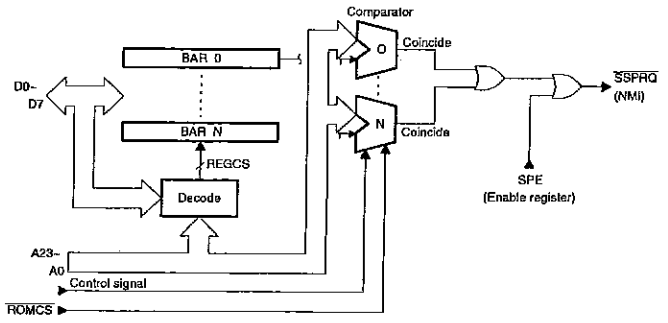


Fig. 6-2

As the address detection system, the brake address register comparison system is employed though the mapping system was employed in the conventional monitor RAM. The address registerlocated in MPCA is always compared with the system address bus to monitor and generate NMI signal at a synchronized timing and togo to NMI exception process.
In the exception process routine service routine, the entry address is checked to go to SSP sub routine.
Entry to the break address register (BAR) is performed through address FFFF00H or later decoded in MPCA5.

2) SSP register

The break address register (BAR) is accessed through direct address of FFFF00H~FFFFFFH. Entry number is 32 entry.

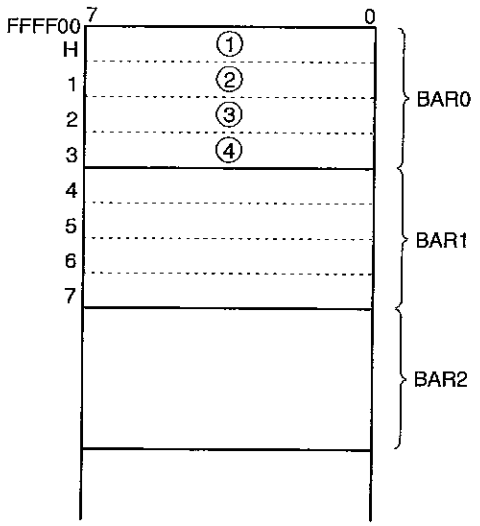
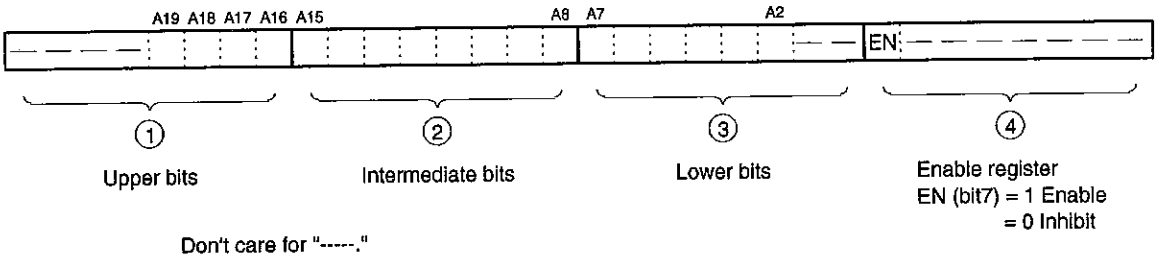


Fig. 6-3

Each BAR is composed of 4 byte address. Bit composition is as follows:



< BAR composition >

Fig. 6-4

④ is the enable register. The entry registers of the break address are assigned to ①, ②, and ③. Each bit of address corresponds to each bit position, writing to ①, ②, and ③ is performed without shifting. The corresponding area is 1MB space of ROS1 and ROS2.

3) SSP register access method

Access to SSP break address register is performed through the temporary register as shown below:

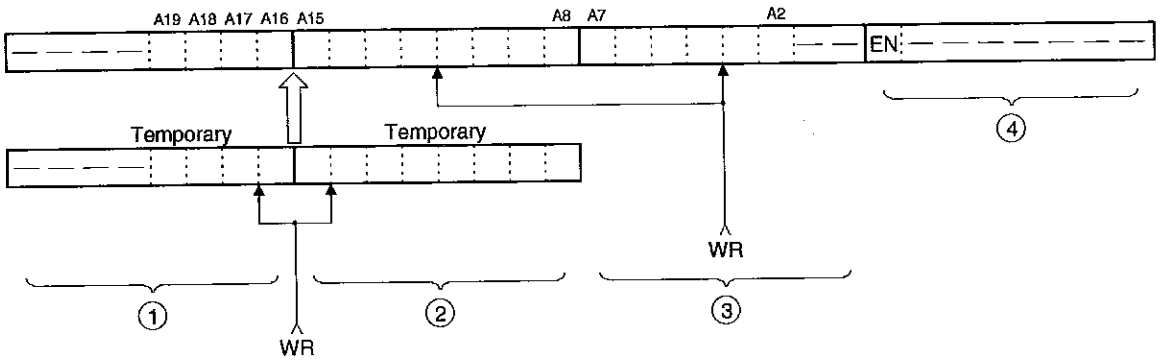


Fig. 6-5

Enable flags can be accessed individually.
Though enable register ④ can be accessed individually, writing to brake address registers ① and ② is performed at the same time as writing to brake address register ③ through the temporary register.
Therefore, set ① and ② to temporary, then write into ③ at last.
Since the temporary register is commonly used by BAR sets, thefollowing register setting is performed after completion ofsetting of each break address register.

③ SSP control method

Access to the enable register and the brake address register is only possible when writing to them from the CPU.

bit 7	6	5	4	3	2	1	0	
0	0	0	CMP4	CMP3	CMP2	CMP1	CMP0	(FFFFFFH)

Information on which brake register the SSP brake is detected in is read as binary data by reading address FFFFFFH (*1).
Used in an expanded register.
Normally is a reserve bit. Whenreading, fixed to 0.

If there are 32 break registers, binary expression is made with the above 5 bits, and 0th is "00000B" and 31st is "11111B."

When detected simultaneously by two or more break registers, onewith the smaller BAR number is read as binary data.

The brake signals (NMI) and the above detection data (CMP0~4) areheld until the above detection data are read. So read should bemade in the NMI sub routine. (Clear by FFFFFFH read.)

* 1: FFFFFFH is not fulldecoded. (FFFF00H~FFFFFFH). Therefore,unnecessary read access in parentheses should not be performed.

7. PRINTER control circuit

1)Block diagram

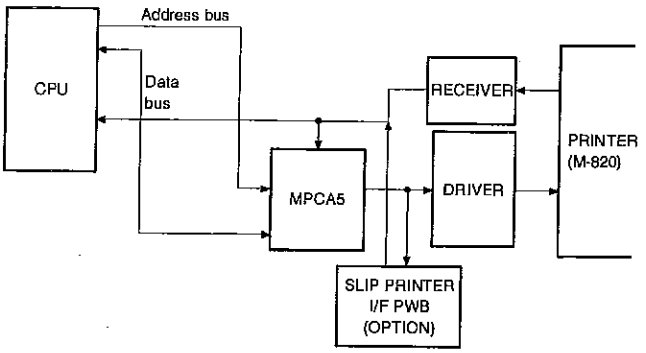


Fig. 7-1

2) General description of the printer controller

The M820 is used as the R/J printer of the body and the M240 is used as the slip printer. The printer mechanical timing control is made by the CPU through MPCA5.

3) Motor drive circuit

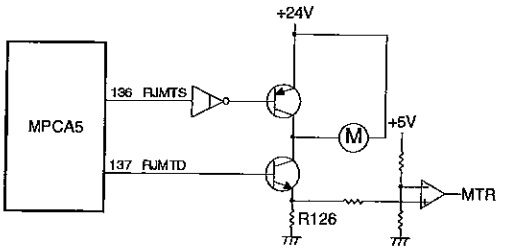
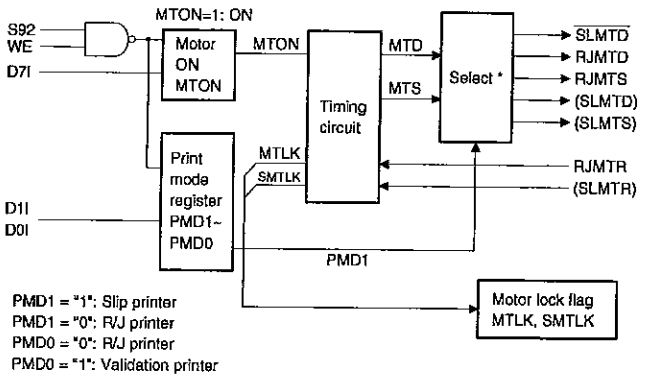


Fig. 7-2



MPCA5 internal circuit

Fig. 7-3

The printer motor ON/OFF control is performed with RJMTD as the drive signal and RJMTS as the brake signal. Motor lock detection is performed as follows:

Check by the hardware: The motor drive current flowing from the MTD transistor is checked across R126. When an overcurrent is detected, the MTR signal becomes HIGH to drive the MTS and MTD signals in the MPCA5 to HIGH impedance to stop conduction of the motor.

When the motor is stopped, the CPU timing pulse width is extended and the CPU judges it as motor lock.

CPU motor lock detection can be read out as internal register MTLK. Lock can be released by writing dummy data into MTLK as well as by conventional hardware reset.

Check by the CPU: When timing pulse from the printer is not generated for more than the specified time, the CPU judges it as motor lock, the MTON is reset (To High) and the motor is stopped.

4) Printhead mechanism

With the timing plus (TS) from the motor, current is applied to the dot wire drive coil to print.

- Discussion is given here to explain how a single dot wire is driven.

① When current is applied to a coil, the actuator moves towards the arrowhead (a) as the steel core is magnetized. The actuator makes connection with the wire, and the wire pushed out towards the platen.

② As the wire hits the platen with the ink ribbon and paper in-between, a dot is then printed.

③ When current is removed from the coil, the actuator and the wire return to their home positions by means of the actuator spring and wire return spring.

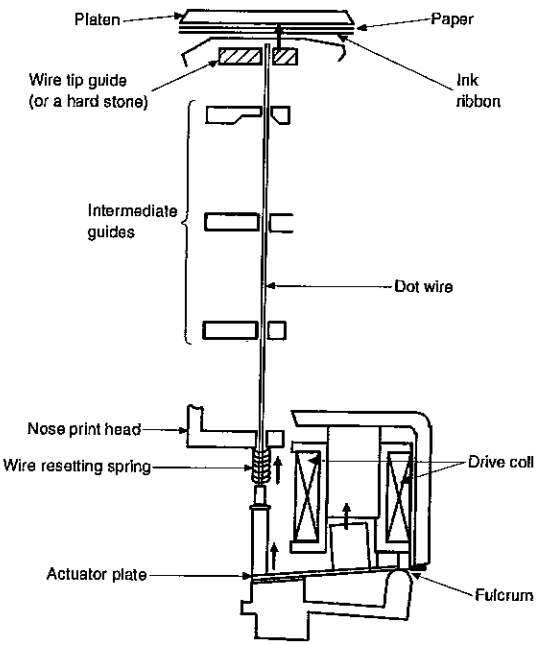
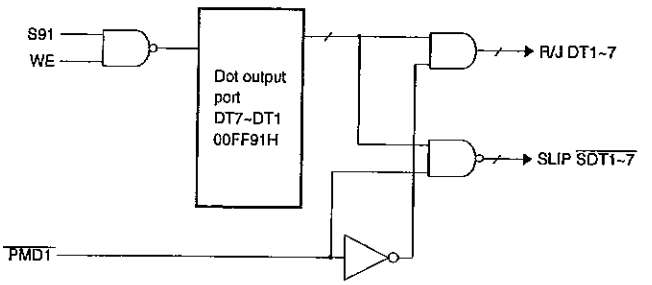


Fig. 7-4

5) Dot wire drive control circuit



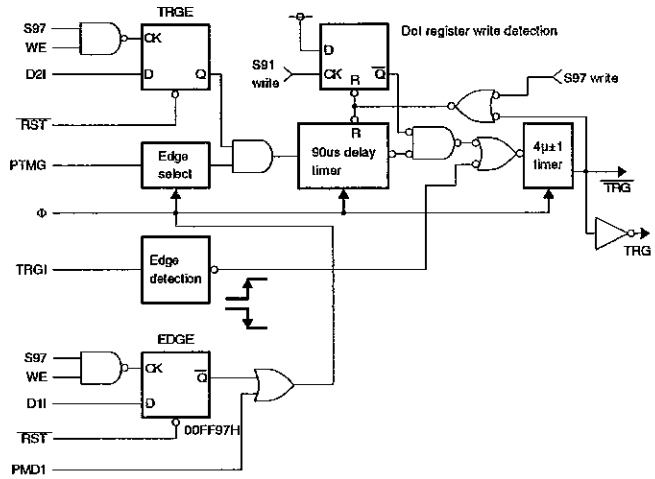
MPCA5 internal circuit

Fig. 7-5

When writing is made into address 00FF91H by the dot register inj MPCA5, dot wire drive signals DT1~DT7 are formed.

When $\overline{PMD1}$ is low, the R/J printer is selected.

6) Print trigger generating circuit



MPCA5 internal circuit
Fig. 7-6

- Automatic trigger mode selection register (TRGE)
  TRGE = 1: Automatic trigger generation
  TRGE = 0: Trigger is generated at change edge of OCRA matchoutput.
  (Reset initial value = 0)
- Timing pulse active edge select register (EDGE)
  EDGE = 0: Falling edge
  EDGE = 1: Rising edge
  (Reset initial value = 0)

7) Dot solenoid drivers (solenoid 1 - 7)

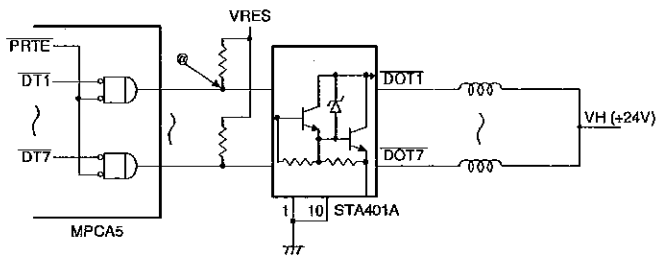


Fig. 7-7

Current to the dot solenoid is controlled in the following manner:

- VRES must be at a high level.
- At the same time $\overline{DTS1}$ is set low, $\overline{TRG}$ must be set low.
- $\overline{PRTE}$ is now set low. (MPCA5)
- PE must be set high level.
- The signal is turned high at point @, the magnet driver output is set low, and then VH flows through the magnet driver.
- The dot wire now protrudes to hit and print.

8) Sensor signal receive circuit

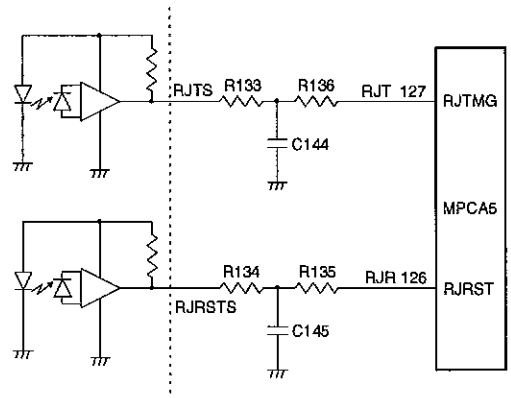
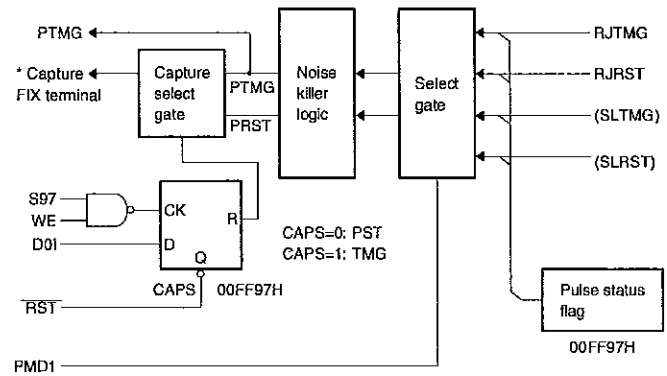


Fig. 7-8
MPCA5 internal circuit



** PRST/PTMG is in the same phase (non-reversion) of RJTMG/RJRST.

Fig. 7-9

The signal from the photocoupler within the printer is converted into TTL level and conveyed to the MPCA5.

9) Paper feed, stamp and cutter circuit

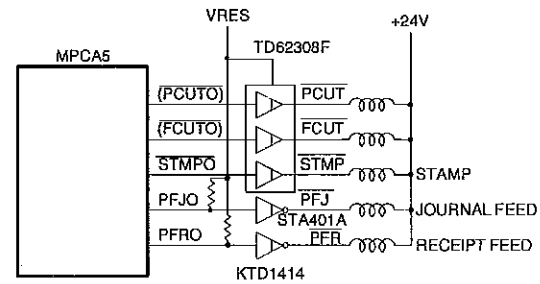


Fig. 7-10

The paper feed/stamp related signals issued from MPCA5 and pulled up by the VRES signal to prevent action when the power supply is not steady.

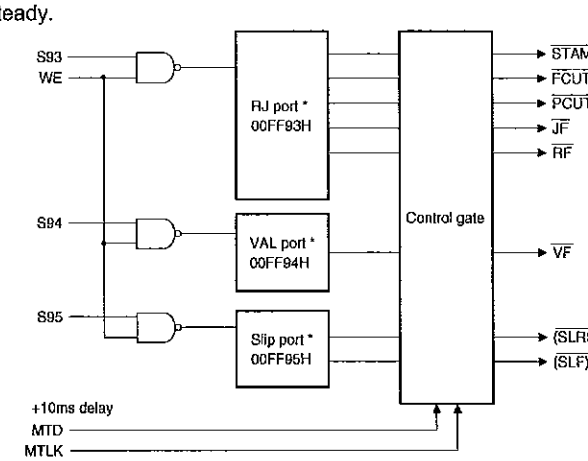


Fig. 7-11

Printer control signals are generated by writing each port address into the register address in PMCA5.

CAUTION

If fuse F2 should be blown, the dot head solenoid may be shorted. Be sure to check the head impedance and driver breakdown.

When fuse F2 is blown:

① Remove F2, and perform the service resetting. The set the mode switch to a position other than SRV and SRV' and turn off the power.

② Install fuse F2 (1.5A)and turn on the power.
If the fuse blows with the above operation, driver STA401A may be shorted.

③ Turn off the power.

④ Disconnect the printer cable from the printer. Measure impedance between the printer body connector pin 21 and the following pins:
18, 20, 24, 25, 28, 29, 30
The impedance must be 12.4 ~ 18Ω.
If impedance is outside the above range, the dot solenoid is bad. Replace the dot head unit.

8. Drawer drive circuit

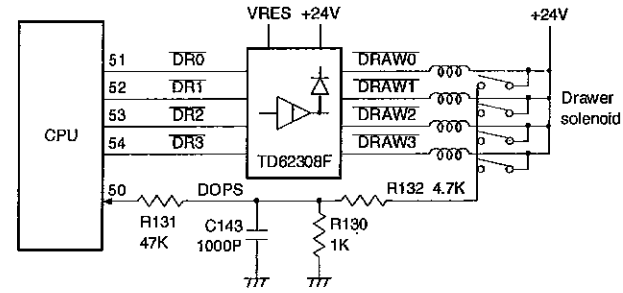
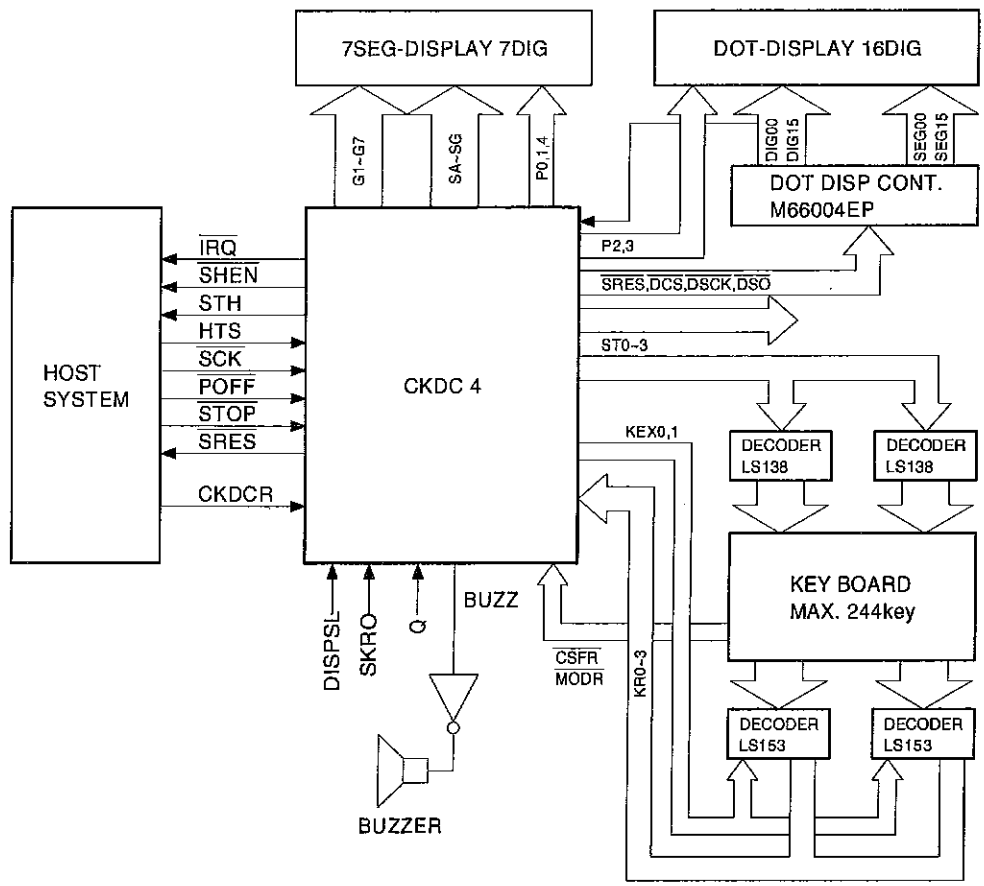


Fig. 8-1

The drawer is directly supported by the CPU. No action starts when the power supply is not steady as the output stage of the driver is pulled VP by VRES signal.
Drawer open and close is sensed with the microswitch provided in the drawer whose signal is level converted with R75 and R77 and directly read by the CPU.

9. Key, display, timer, buzzer controls

The keys, switches, displays, timer/calendar, and buzzer are controlled by the CKDC-4 on the display PWB.



Block diagram
Fig. 9-1

1) Power on/off sequence

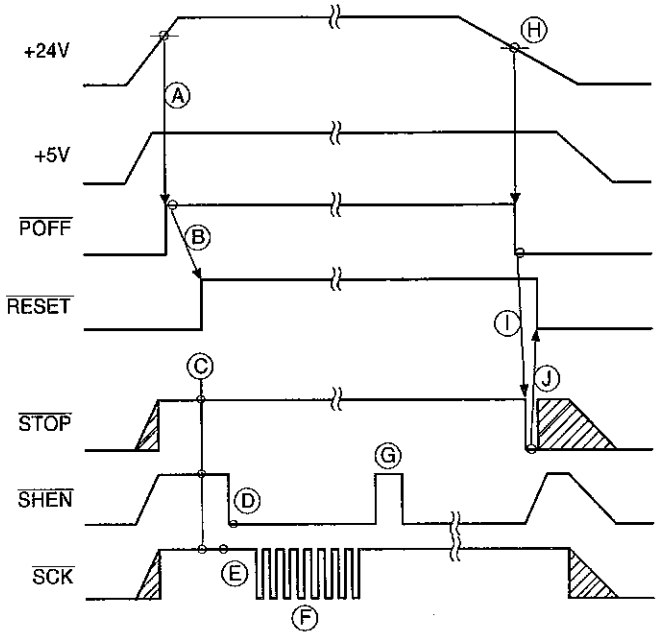


Fig. 9-2

Hatched area indicates logic unstable.

<At power on>

When +24V power rises, the signal POFF is forced high (A), by which time the +5V supply becomes stable. The CKDC-III monitors the state of POFF while updating the timer/calendar in the low power standby mode, and when the high state of POFF is detected, the system reset signal (RESET) is set high (B), by which time the output lines STOP and SCK of the CPU and MPCA5 have been initialized to high, respectively (C). Thereafter, the CKDC-III sets SHEN active (low) (D) to notify the CPU of the command/data communication ready state.
One byte data/command can be transferred with eight SCK pulses (F). When one byte has been transferred with eight SCK pulses, the CKDC-III sets SHEN high to initiate internal processing. After completion of the internal processing, when the next byte transfer becomes ready, the CKDC-III sets SHEN back to a low state to wait for the next byte transfer (G).
Thereafter, the SHEN and SCK timing described above is repeated to carry on the communication.

<At power off>

When +24V power drops, POFF goes low (H).
A low on the POFF line causes a low level interrupt request which is sent the IRQ0 pin of the CPU. Within a maximum of 10msec of the low level IRQ0 input, the CPU performs software processing necessary for power-off, after which the STOP output is set low (I).
When STOP goes low, the CKDC-III sets RESET low to reset the whole system (J). And, the +5V supply is held at 4.75V or higher voltage, after which the voltage drops to a level that the logic circuit does not operate.

2) Key and switch scanning

Strobes ST0 ~ ST3 are decoded on the keyboard by two 74LS138 3-to-8 decoders to generate 16 strobe signals of S15 ~ S0.
The key matrix consists of 16 strobe lines and 16 returns lines of KR0A, KR1A, KR2A, KR3A, KR0B, KR1B, KR2B, and KR3B.
To minimize interfacing lines between the CKDCIII and the keyboard unit, two multiplexers (74HC153) are used to multiplex signals by the timing controlled with the signals KEX0 and KEX1 which are sent to the CKDCIII on the return lines of KR0 ~ KR3.

Timing ST

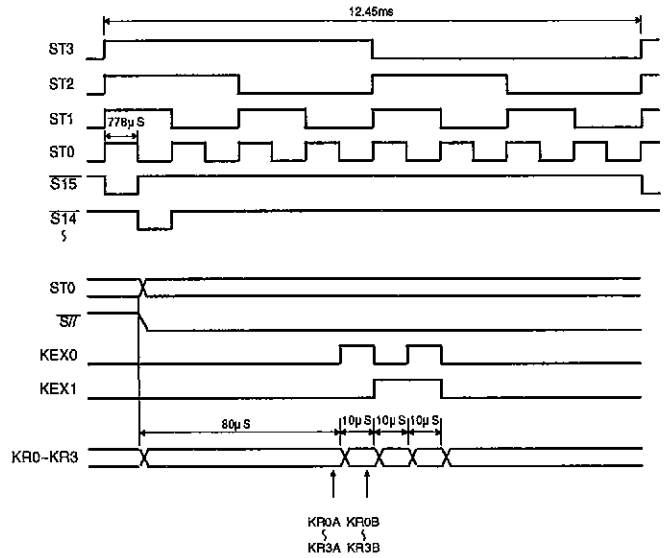


Fig. 9-3

The mode switch in provided with a special return line MODR, apart from the above return lines.
In the same manner, the clerk, paper feed key (J/R), and receipt on/off switches use CFSR as the return line.

3) DISPLAY CONTROL

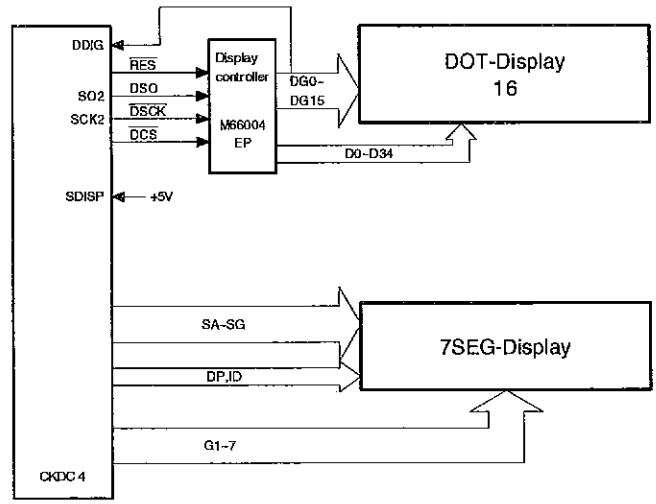


Fig. 9-4

CKDC4 directly drives the 7-segment display unit and the dot display is driven via M66004FP.

<7-segment display>

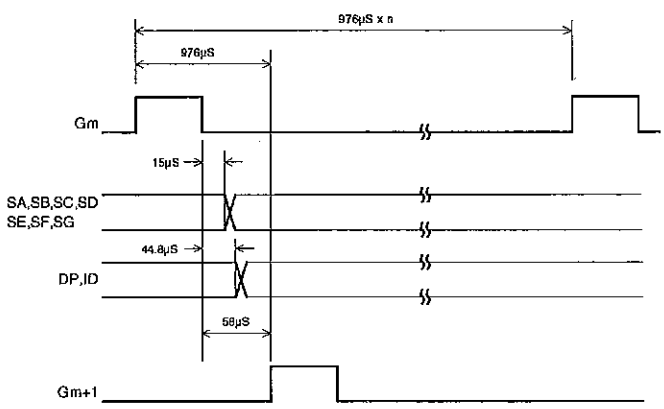


Fig. 9-5

<Dot display>

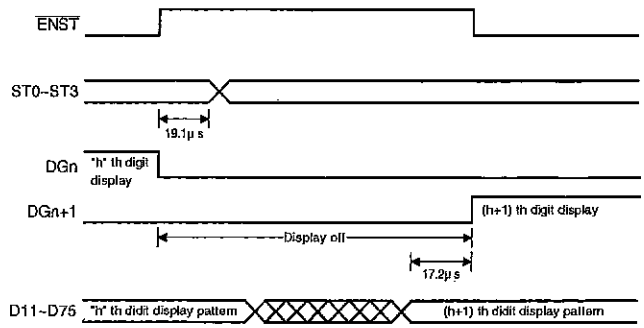


Fig. 9-6

IMPORTANT:

The CKDCIII lines are not high voltage resistive ports. Damage may occur to the CKDC4 if lines are ahorted carelessly when using oscilloscope probes.

- Dot matrix tube
  A 4-bit binary output signals (ST0-ST3) from CDKC4 are converted into the digit drive signal (DG0-DG15) in the M66004FP.

<Dot display control>

The CKDC4 controls the character segment (5 x 7) and the indicator of the dot display by using the controller (M66004FP) for dot display control.

① M66004PF/Dot display control signal

Signal name	Contents	Pin/Remark
DSO	Serial data output signal for M66004FP	C-MOS pin
$\overline{DSCK}$	Serial shift clock output signal for M66004FP	C-MOS pin. Requires to be pulled up
$\overline{DCS}$	Chip select output signal for M66004FP	C-MOS pin

D0	D1	D2	D3	D4
D5	D6	D7	D8	D9
D10	D11	D12	D13	D14
D15	D16	D17	D18	D19
D20	D21	D22	D23	D24
D25	D26	D27	D28	D29
D30	D31	D32	D33	D34

10. Power supply circuit

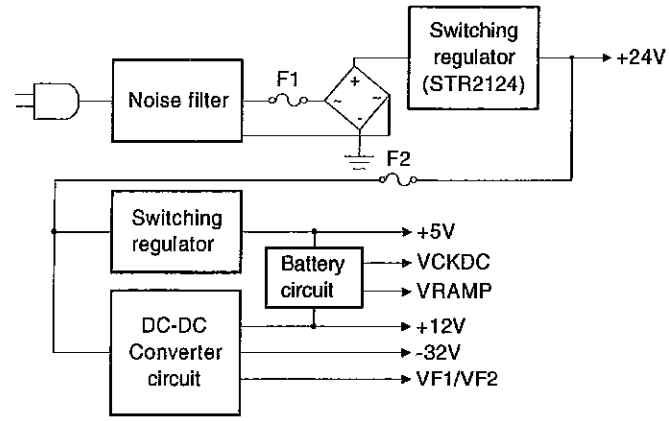


Fig. 10-1

+24V:	Printer, solenoid power
+5V:	VCC (Logic power)
+12V:	Battery charge, IN-LINE driver power
–32V:	Display tube power
VF1, VF2:	Display tube power (AC)
VRAM:	Battery back-uped power
VCKDC:	CKDC III Back-up power

For the DC-DC converter, refer to section 8 of cash register Basic manual.

11. Switching regulator circuit

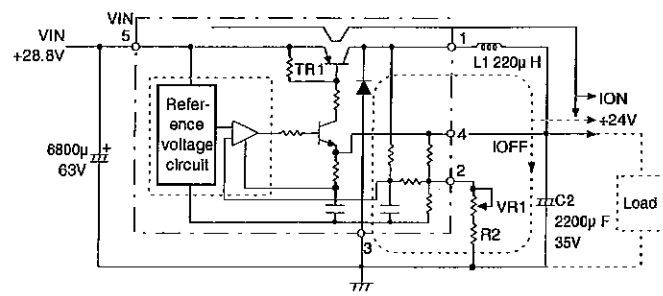


Fig. 11-1

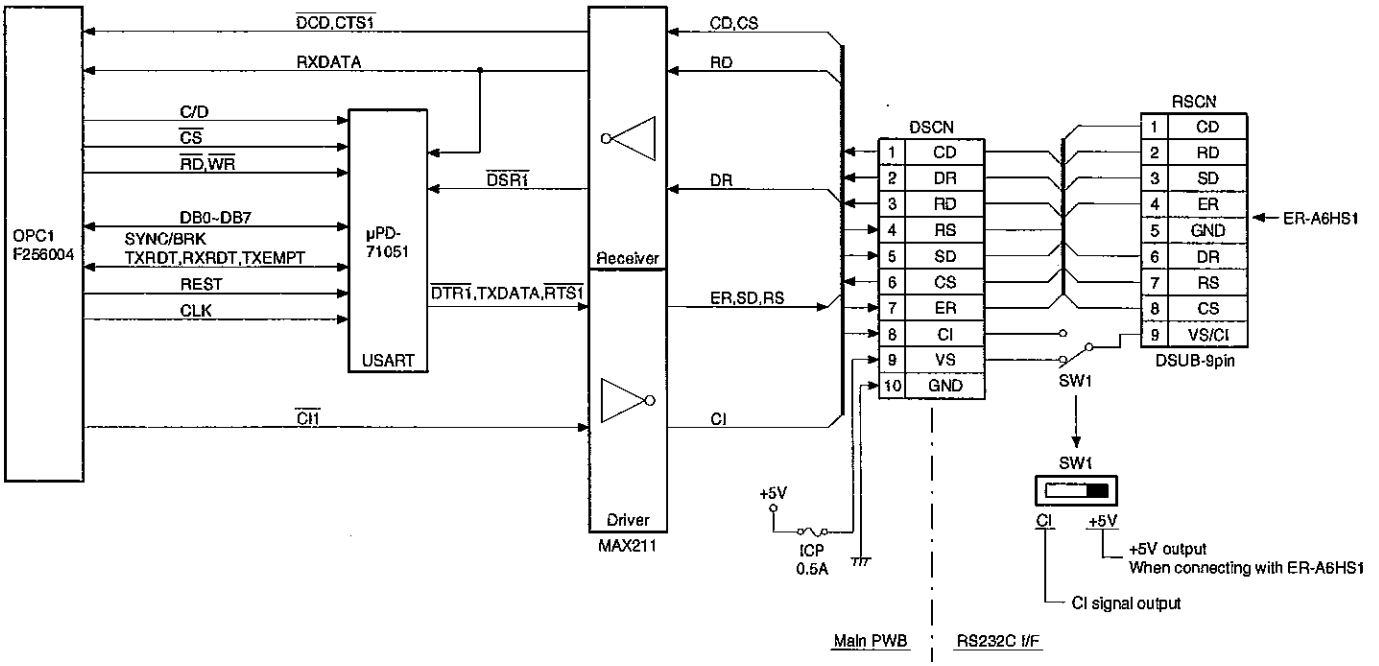
By switching VIN (+28.8V) by the transistor TR1 within the STR2124, DC+24V supply is obtained through the LC network. Stable +24V is obtained by controlling on/off duty of TR1.

ION: Current when TR1 is on.
IOFF: Current when TR1 is off.

12. Scanner interface

The ER-A610 includes the RS-232 interface which has the power supply function to the hand scanner (ER-A6HS1) as a standard provision.

1) Block diagram



When the ER-A6HS1 is connected, +5V power is supplied to Pin 9 of the RS-232 connector.
SW1 on the RS-232 interface allows switching of the VS signal (+5V) and the CI signal.

CAUTION
A current of 100mA flows through the DSCN connector 8 pin.
If a current of 500mA or more flows even in a moment, ICP 0.5A is opened.

2) Description of main LSI

2)-1. OPC1 (F256004PJ)

① General description

The OPC1 is a gate array of integrated peripheral circuits of RS-232/Simple IRC interface.
One chip of the OPC1 is equipped with four communication circuits. (Three of them are for RS-232 only: UNIT 0 ~ 2, one is for selection of simple IRC/RS-232: UNIT 3)
The ER-A610 uses UNIT3 (RS-232 interface).

UNIT NO.	Purpose	ER-A610
UNIT0	RS-232	Not used.
UNIT1	RS-232	Not used.
UNIT2	RS-232	Not used.
UNIT3	RS-232/Simple IRC	Used.

Each UNIT of the OPC1 has the following functions:

① Timer function
Used for the timer between characters in data reception.

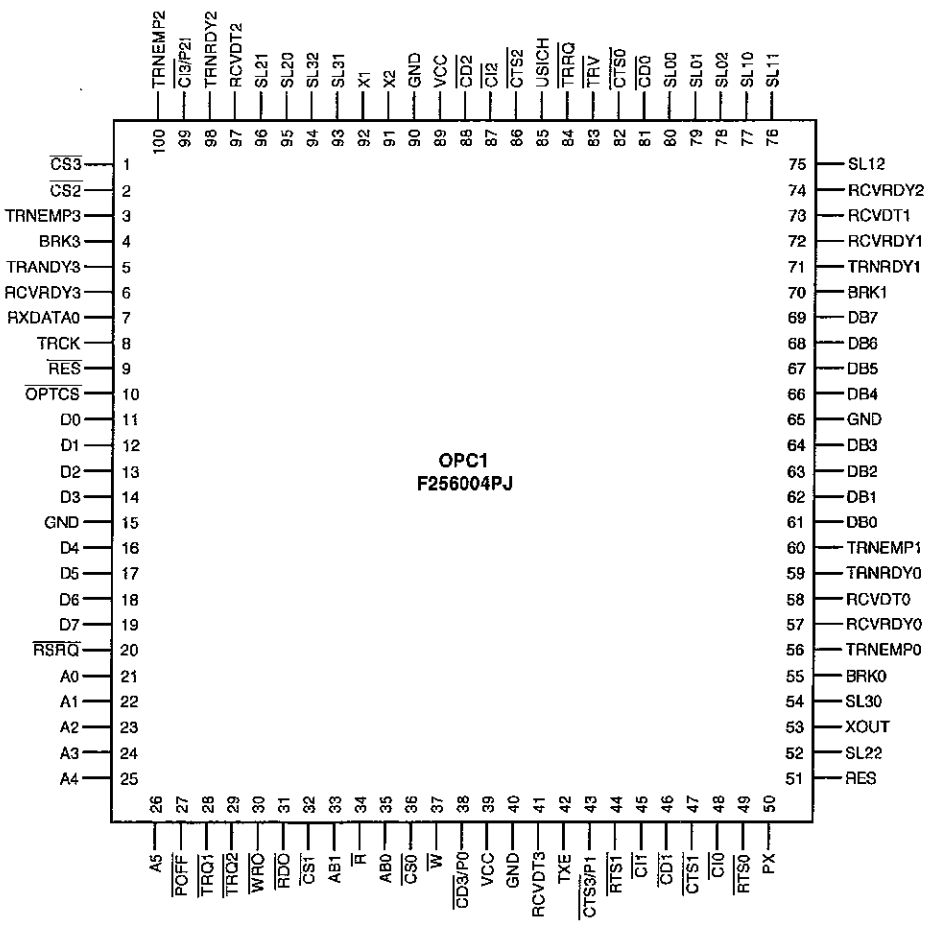
② Address decode
USART chip select output and own select.

③ Interruption control
$\overline{RSRQ}$, $\overline{TRRQ}$ output using outputs from USART (TRNRDY, TRNEMP, RCVRDY, BRK) and RS-232 control signals ($\overline{CI}$, $\overline{CTS}$, $\overline{CD}$) as interruption factors.
(For the simple IRC, TRNEMP is excluded.)

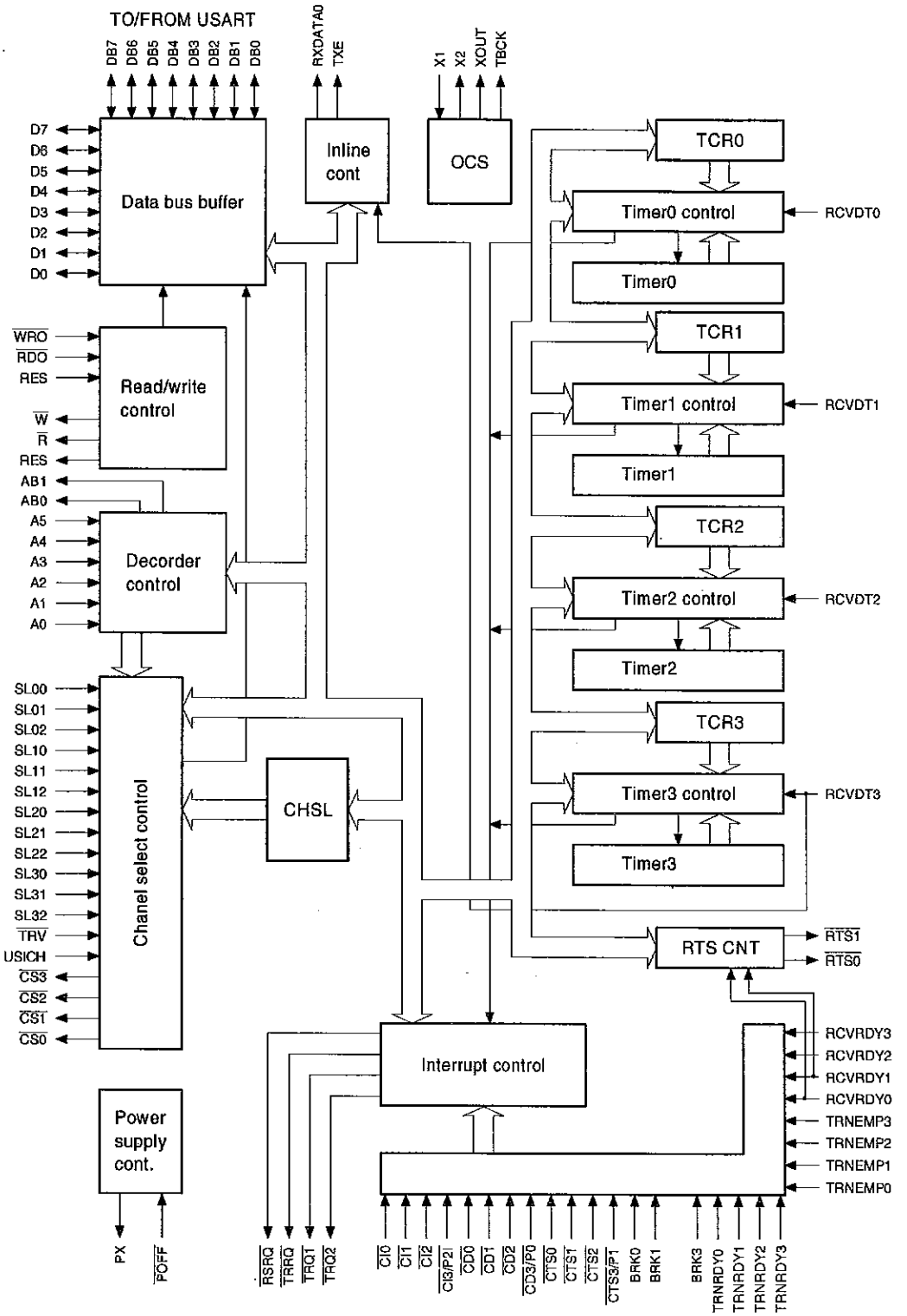
* $\overline{RSRQ}$: For RS-232
$\overline{TRRQ}$(Not used): For simple IRC

④ Simple IRC send/receive control (UNIT3 only) : Not used

② Pin configuration



③ Block diagram



④ Pin description

OPC1 pin table

The signals marked with "-" at the end are LOW active signals. Example: "CS1-" = "$\overline{CS1}$"

No.	Pin No.	Pin name	I/O	Pin	ER-A610	Description
1	80	SL00	I	ICU	GND	RS-232/UNIT0 channel select
2	79	SL01	I	ICU	GND	
3	78	SL02	I	ICU	GND	
4	77	SL10	I	ICU	GND	RS-232/UNIT1 channel select
5	76	SL11	I	ICU	GND	
6	75	SL12	I	ICU	GND	
7	95	SL20	I	ICU	GND	RS-232/UNIT2 channel select
8	96	SL21	I	ICU	GND	
9	52	SL22	I	ICU	GND	
10	54	SL30	I	ICU	+5V	RS-232/UNIT3 channel select
11	93	SL31	I	ICU	GND	
12	94	SL32	I	ICU	GND	
13	36	CS0-	O	O	NC	RS-232 USART chip select
14	32	CS1-	O	O	NC	
15	2	CS2-	O	O	NC	
16	1	CS3-	O	O	/CS	RS-232/INLINE USART chip select
17	81	CD0-	I	IS	+5V	RS-232 control signal CD- input
18	46	CD1-	I	IS	+5V	
19	88	CD2-	I	IS	+5V	
20	38	CD3-/P0-	I	IS	/DCD1	RS-232 CD-/INLINE P0-
21	82	CTS0-	I	IS	+5V	RS-232 control signal CTS- input
22	47	CTS1-	I	IS	+5V	
23	86	CTS2-	I	IS	+5V	
24	43	CTS3-/P1-	I	IS	/CTS1	RS-232 CTS-/INLINE P1-
25	48	CI0-	I	IS	+5V	RS-232 control signal CI- input
26	45	CI1-	I	IS	+5V	
27	87	CI2-	I	IS	+5V	
28	99	CI3-/P2I	I	IS	/DSR1	RS-232 CI-/INLINE P2I
29	55	BRK0	I	ISC	GND	RS-232 USART BREAK signal
30	70	BRK1	I	ISC	GND	
31	27	POFF-	I	IS	/POFF	POFF signal (LOW: P-OFF, HIGH: P-ON)
32	4	BRK3	I	IS	SYNC/BRK	RS-232/INLINE USART BREAK signal
33	57	RCVRDY0	I	ISC	GND	RS-232 USART RCVRDY signal
34	72	RCVRDY1	I	ISC	GND	
35	74	RCVRDY2	I	ISC	GND	
36	6	RCVRDY3	I	IS	RXRDT	RS-232/INLINE USART RCVRDY signal
37	59	TRNRDY0	I	ISC	GND	RS-232 USART TRNRDY signal
38	71	TRNRDY1	I	ISC	GND	
39	98	TRNRDY2	I	ISC	GND	
40	5	TRNRDY3	I	IS	TXRDT	RS-232/INLINE USART TRNRDY signal
41	56	TRNEMP0	I	ISC	GND	RS-232 USART TRNEMP signal
42	60	TRNEMP1	I	ISC	GND	
43	100	TRNEMP2	I	ISC	GND	
44	3	TRNEMP3	I	IS	TXEMPT	RS-232/INLINE USART TRNEMP signal
45	58	RCVDT0	I	ISC	+5V	RS-232 RCVDT signal (LOW: TIMER START)
46	73	RCVDT1	I	ISC	+5V	
47	97	RCVDT2	I	ISC	+5V	
48	41	RCVDT3	I	IS	RXDATA	RS-232/INLINE RCVDT signal
49	20	RSRQ-	O	3S	/IRQ2	RS-232 IRQ- signal
50	83	TRV-	I	ISC	+5V	INLINE YES/NO
51	7	RXDATA0	O	O	NC	INLINE RXDATA OUT
52	42	TXE	O	O	NC	INLINE TRNS ENABLE
53	84	TRRQ-	O	3S	NC	INLINE IRQ- signal
54	28	TRQ1-	O	3S	/TRQ1	TIMER IRQ signal (RS-232)

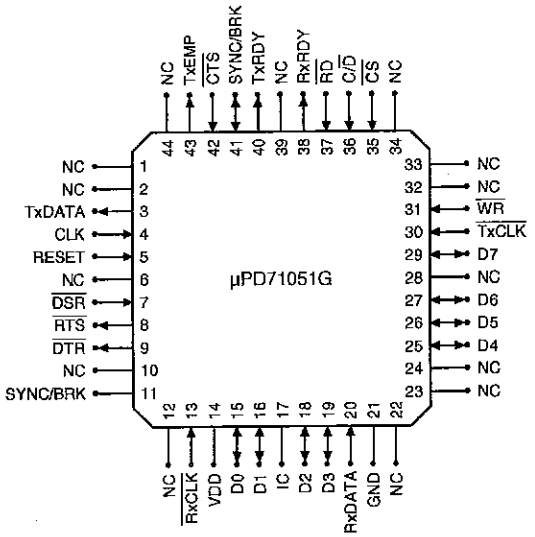
No.	Pin No.	Pin name	I/O	Pin	ER-A610	Description
55	29	TRQ2-	O	3S	NC	TIMER IRQ signal (INLINE)
56	11	D0	I/O	IOU	D0	DATA BUS (MAIN)
57	12	D1	I/O	IOU	D1	
58	13	D2	I/O	IOU	D2	
59	14	D3	I/O	IOU	D3	
60	16	D4	I/O	IOU	D4	
61	17	D5	I/O	IOU	D5	
62	18	D6	I/O	IOU	D6	
63	19	D7	I/O	IOU	D7	
64	61	DB0	I/O	IOU	DB0	DATA BUS (USART)
65	62	DB1	I/O	IOU	DB1	
66	63	DB2	I/O	IOU	DB2	
67	64	DB3	I/O	IOU	DB3	
68	66	DB4	I/O	IOU	DB4	
69	67	DB5	I/O	IOU	DB5	
70	68	DB6	I/O	IOU	DB6	
71	69	DB7	I/O	IOU	DB7	
72	21	A0	I	I	A0	ADDRESS BUS (MAIN)
73	22	A1	I	I	A1	
74	23	A2	I	I	A2	
75	24	A3	I	I	A3	
76	25	A4	I	I	A4	
77	26	A5	I	I	A5	
78	10	OPTCS-	I	I	/OPTCS	OPTION CHIP SELECT (from MAIN)
79	31	RDO-	I	I	/RDO	READ signal (from MAIN)
80	30	WRO-	I	I	/WRO	WRITE signal (from MAIN)
81	9	RES-	I	IS	/RES	RESET signal (from MAIN)
82	34	R-	O	O	/RD	READ signal (To USART)
83	37	W-	O	O	/WR	WRITE signal (To USART)
84	51	RES	O	O	RES	RESET signal (To USART)
85	92	X1	O		NC	cillation circuit
86	91	X2	I		X2	
87	53	XOUT	O	O	XOUT	Clock for USART
88	8	TRCK	O	O	/TXCLK	T/R clock for 1CH USART
89	35	AB0	O	O	C/$\overline{D}$	ddress bus for USART (COMMAND or DATA SELECT)
90	33	AB1	O	O	NC	
91	85	USICH	I	ISC	+5V	UNIT3 USART 1CH/2CH select
92	50	PX		O	NC	Power source clock
93	39	VCC			+5V	
94	89	VCC			+5V	
95	15	GND			GND	
96	40	GND			GND	
97	65	GND			GND	
98	90	GND			GND	
99	49	RTS0-	O	O	NC	RS-232 control signal RTS- output
100	44	RTS1-	O	O	NC	

ICU : CMOS level input (internal pullup resistor)
O : Output
IS : TTL level input (internal schmit circuit)
ISC : CMOS level input (internal schmit circuit)
3S : Three state output
IOU : I/O port (internal pullup resistor)

2)-2. Transmission Controller 71051G (USART)

The 7051G is a Universal Synchronous/Asynchronous Receiver/ Transmitter (USART) Chip designed for data communications in microcomputer systems. The USART is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use. The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously it can receive a serial data stream and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it has received a character for the CPU. The CPU can read the complete status of the USART at any time. These include data transmission errors and control signals such as SYNC/BRK, TxEMPT.

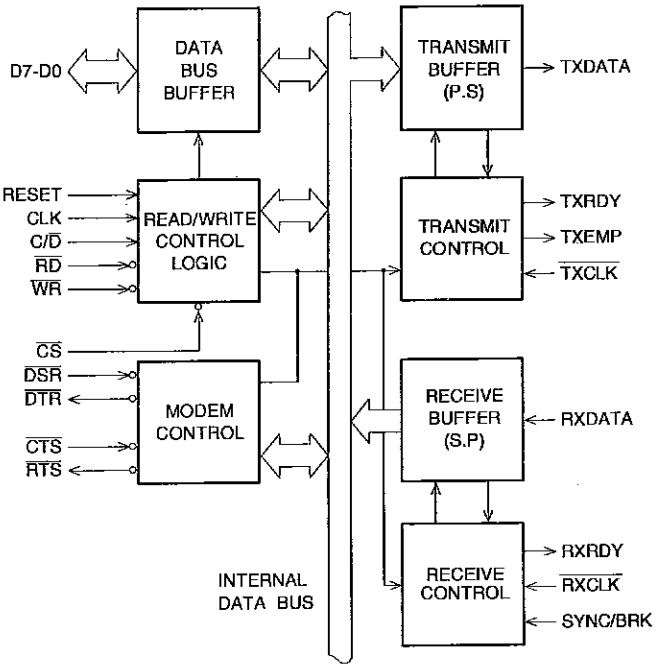
① PIN CONFIGURATION



② PIN DESCRIPTION

Pin name	Description
D0-D7	Data bus (8bits)
TXDATA	Transmitter data
$\overline{\text{TXCLK}}$	Transmitter clock
TXRDY	Transmitter ready
TXEMP	Transmitter empty
RXDATA	Receiver data
$\overline{\text{RXCLK}}$	Receiver clock
RXRDY	Receiver ready
CLK	Clock pulse
RESET	Reset
$\overline{\text{DSR}}$	Data set ready
$\overline{\text{RTS}}$	Request to send data
$\overline{\text{DTR}}$	Data terminal ready
WR	Write data
$\overline{\text{CS}}$	Chip enable
C/$\overline{\text{D}}$	Control or data is to be written or read
$\overline{\text{RD}}$	Read data
SYNC/BRK	Break
VDD	+5V

③ BLOCK DIAGRAM



CHAPTER 5. TEST FUNCTION

1. General

1) This diagnostic program has been developed for diagnosing machine functions in the field. The program is contained with in the ER-A610.
The diagnostic program is stored in the external ROM which will be executed by the CPU (H8/510) which requires the following diagnostic operations:

a) Proper power supply voltages are mandatory for logic circuits (+5V, VRAM, VCKDC, POFF, 12V, +24V).

b) CPU input/output pins, CPU internal logic, CKDC4, MPCA5, TPRC, address decoder, address bus, data bus, and common ROM/RAM must be working properly.

2. Operational procedure

To start the diagnostic program, you must enter the following command.
3-digit test item number → [CA/AT] key in the SRV mode.
The key assignment must be properly set and a part for ROM and RAM must be operating properly to go into this mode because the control jumps to the program area in the SRV mode. A master reset must be performed before operating the ECR for the first time. After any option is installed, a program reset is required. When the master reset or program reset is performed, be sure to check the printout on the journal paper.

Master reset: Turn power on in the SRV' mode and change it to the SRV mode with the [CA/AT] key pressed.
Journal print: MASTER RESET ***
Program reset: Turn power on in the SRV' mode and change it to the SRV mode.
Journal print: PRG. RESET ***

3. Test command list

With the SRV mode and the following command entry, the test starts.

Code	Description
100	Display test-1
101	Key, server, and switch position code display
102	R/J printer test
103	Slip printer test
104	Keyboard test
105	Mode switch test
106	Validation sensor and near end sensor test
107	BOF, TOF and IFV test
108	Calendar oscillator test
109	SSP test
110	Drawer-1 open and sensor test
111	Drawer-2 open and sensor test
112	Drawer-3 open and sensor test
113	Drawer-4 open and sensor test
116	Display test-2
117	SIO test-1
120	Standard RAM test
130	Standard ROM test
150	R/J printer dot pulse width adjustment
200 ~ 206	Option RAM chip test
300 ~ 306	Option RAM address test
400	Option ROM test
500	RS-232 Channel check
501	RS-232 Channel 1 check

[1] Display test-1

① Key operation
100 → [CA/AT]

② Functional description
The following is displayed:

DOT DISPLAY : 0123456789:AaBbC

POP-UP DISPLAY: 4,5,6,7,8,9,-,

③ Check the following items:

a) Check for proper activation of display elements.

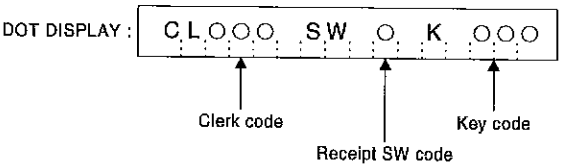
b) Check for blur, uneven illumination, and partial omission.

④ Test termination
Press any key. The test terminates with the test and message printed.

100
Test termination print

[2] Key, cashier, and switch position code display

① Key operation
101 → [CA/AT]



② Functional description
Key, clerk, and receipt switch codes are displayed.

③ Check the following items:
Change key and switch positions for proper display activation.
Server code: 1 hole server key
000 (off state)
001 (Server 1)
002 (Server 2)
~
255 (Server 255)
Receipt switch code: 2 (on state) 3 (off state)
Key code: --- (simultaneous two key) depression, invalid entry)
001 ~ 126

NOTE: Refer to JOB#104, key soft code, for the key code. (Fig. 3-2.)

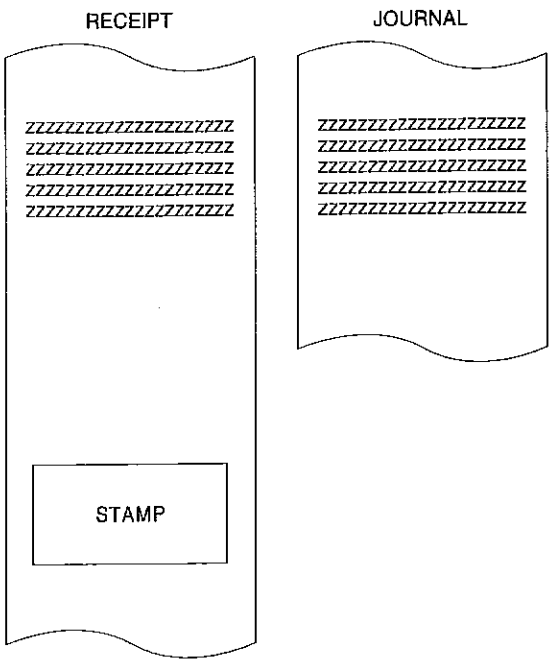
④ Test termination
Change the MODE switch position other than SRV position to terminate the test. The test termination message is printed.

101
Test termination print

[3] R/J printer test

① Key operation
102 → CA/AT

② Content
Five lines of "Z" characters are printed as follows on the receipt and the journal regardless of receipt (ON/OFF) switch setting.



③ Check content

1. Check that the slanted lines of "Z" characters are clearly printed.
2. Check that the characters are printed at a uniform density.
3. Check the paper feed operation and the logo print.
4. Check partial cut and full cut.

④ Termination
This check is terminated automatically.
The termination print is not performed.

[4] Slip printer test

① Key operation
As slip must be set on the print table.
103 → CA/AT

② Functional description
Regardless of paper setting, 35 digits of "Z" are printed on five lines, then the printer stops after releasing the paper.

③ Check the following items:
a) Print starting position must line up in the same column.
b) Check the print quality.
c) Make sure that the paper is released at the terminattion.

<Print sample>

ZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZ
ZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZ
ZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZ
ZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZ
ZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZZ

④ Test termination
The test terminates automatically. If the paper release lever is not up, perform JOB#107 BTF, IFV test to release the paper.

If the ER-33SP (printer and I/F PWB unit) is not connected when performing this test, the following error display is made.
To cancel the error state, press any key or shift the mode key position, and the R/J printer will print the error print, terminating the operation.

Error display:

DOT DISPLAY : SLIP I/F ERR

Error print:

R/J printer: E-----103

[5] Keyboard test

① Key operation
104 → CA/AT

② Functional description
Key actions of the standard version ER-A610 are tested.
Press keys on the keyboard in the order given in the figure 3-1. If the test has been successful, the test terminates with the printout showing correct action of every key. If an error has occured in the course of a test, an error message will be printed immediately upon occurrence of the error. When the test is interrupted, the normal test termination printout is not produced.

③ Check the termination print

④ Test termination
When the last key (see next page) is depressed, the test terminates with the termination printout.

104 | E--✱✱✱ 104

Test termination print | Error print

✱✱✱: Key code that caused the error

(Additional description on the program specifications)
When an error occurs during check, the operation is not terminated and the key to be checked on the key table is not incremented and is kept at standby state for being checked.
To terminate compulsorily, press the END key (at the right bottom). In this case also, the error print is not made.
The display specification is as follows:

DOT DISPLAY : KEY-BOARD OOO

Key code

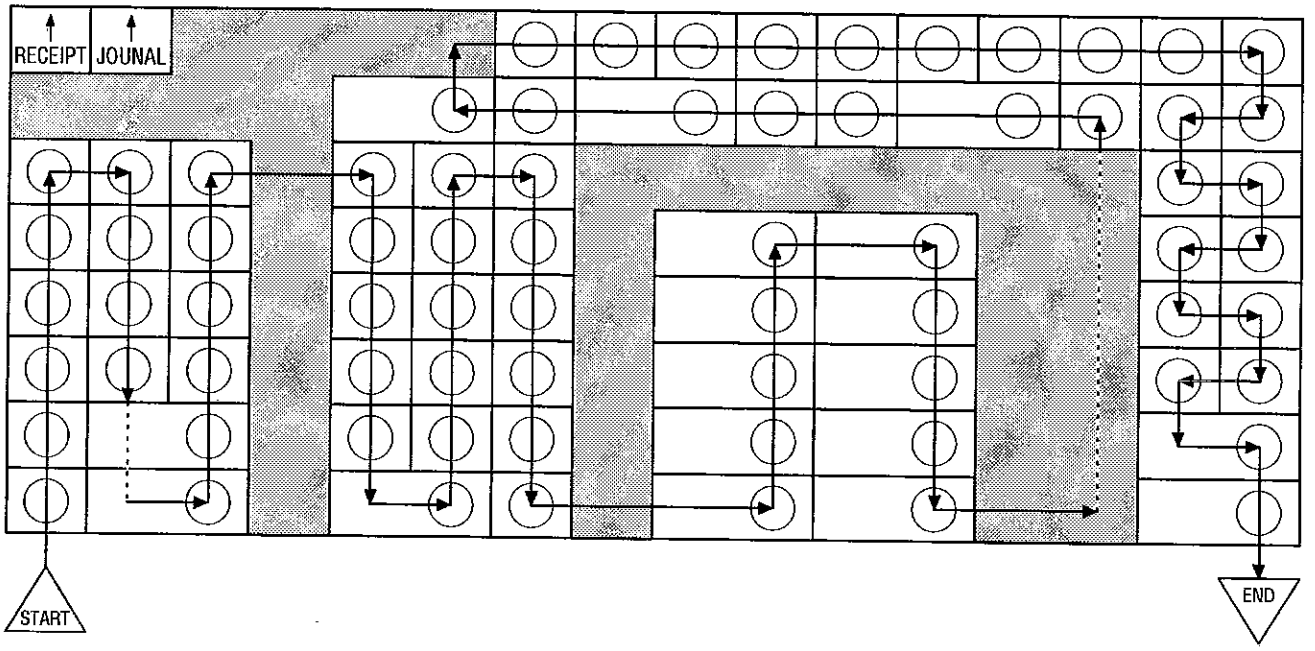


Fig. 3-1: TEST SEQUENSE

RECEIPT	JOUNAL	22	30	38	46	54	62	70	78	86	94	102	110	118	126
7	14	21	29	37	45	53	61	69	77	85	93	101	109	117	125
6	13	20	28	36	44	52	60	68	76	84	92	100	108	116	124
5	12	19	27	35	43	51	59	67	75	83	91	99	107	115	123
4	11	18	26	34	42	50	58	66	74	82	90	98	106	114	122
3	10	17	25	33	41	49	57	65	73	81	89	97	105	113	121
2	9	16	24	32	40	48	56	64	72	80	88	96	104	112	120
1	8	15	23	31	39	47	55	63	71	79	87	95	103	111	119

Fig. 3-2: KEY CODE TABLE

[5] Mode switch test

① Key operation
105 → CA/AT

② Functional description
This test is applicable for checking of the MODE switch. The MODE switch must be changed as described below to do the test.
Initial state mode: SRV mode
Mode check
Change the MODE switch position in the order given below starting from the SRV position.

DOT DISPLAY : M O D E S W I T C H X

X: 0~7,E,F

Mode:	SRV	PGM2	PGM1	OFF	OP X/Z	REG
X :	0	1	2	(E)	3	4

SRV	X2/Z2	X1/Z1	MGR
0	7	6	5

(X: E-intermediate position, F-multiple errors)

When the mode key settings in the sequence other than specified is met or when any key pushed, the program execution will terminate immediately upon occurrence, with the error printout produced, except for the mode switch in the middle position. To avoid this, the mode switch must be rotated correctly. Because nothing is interrogated until the mode key returns to the SRV position once after the switch has turned to the "X2/Z2" positions, it needs not to be rotated slowly.

③ Check the following items:
Check to see if the following are displayed and that the termination print is produced

④ Test termination
When the test has been completed according to the given procedure, the test automatically terminates with the termination message printed. To terminate the test in the middle of an operation, merely depress any key, then, the test will terminate with the error message printed. When an error was encountered, the test automatically terminates with the error message printed on the printer.

105	E - - - - 105
Test termination print	Error print (any key depression)

[6] Validation sensor and near end sensor test

The validation sensor and the near end sensor are optional units.

① Key operation
106 → CA/AT

② Functional description
State of the validation and near end sensor is sensed and displayed.

③ Check the following items:
On and off actions of the validation and near end sensors are tested and their results are displayed.
ON/OFF check is performed for VDS and NES and the display is checked.

DOT DISPLAY : V D S x y N E S z

x: State of the VDSR sensor
y: State of the VDSJ sensor
z: State of the NES sensor

Display	X/Y/Z	Description
VDSR	O	Validation sensor (JOURNAL) not detected
	C	Validation sensor (JOURNAL) detected
VDSJ	O	Validation sensor (RECEIPT) not detected
	C	Validation sensor (RECEIPT) detected
NES	O	Journal side paper roll near end detected.
	C	Journal side paper roll near end not detected.

NOTE: "C" is always displayed when no sensor is used.

④ Test termination
Any key depression causes the test to terminate with the termination message on printout.

106
Test termination print

[7] BOF, TOF and IFV test

① Key operation
107 → CA/AT

② Functional description
After releasing the paper, the state of BOF, TOF, and IFV sensor are sensed and displayed.

③ Check the following items:
BOF, TOF: Check the paper set condition.
IFV: Check the connection of the ER-31SP slip printer and slip printer interface.
Check the on and off actions.

DOT DISPLAY : I F V z B T F x y

x: State of IFV
y: State of the BOF sensor
z: State of the TOF sensor

Display	x/y	Description
IFV	O	Slip printer or slip printer interface not in connection
	C	Slip printer or slip printer interface connection
BOF	O	Slip paper not detected
	C	Slip paper detected
TOF	O	Slip paper not detected
	C	Slip paper detected

④ Test termination
Any key depression terminates the test with the termination print.

107
Test termination print

Note 1: Before performing this test, connect the slip printer and the slip printer I/F. If not, "SLIP I/F ERR" occurs.
Note 2: Before turning on/off the connector for IFV checking, be sure to set the mode to other than SRV and turn off the power.

[8] Calendar oscillator test

① Key operation
108 → CA/AT
Functional description
This program is used to test the calendar oscillator function.

DOT DISPLAY : T I M E R C H E C K

POP UP DISPLAY : * * - * *

-: Present time

② Check the following items:
i) Testing blinking "-". (500ms ON and OFF)

③ Test termination
Any key depression terminates the test with the termination print.

108
Test termination print

[9] SSP test

① Key operation
109 → CA/AT

② Functional description
If an SSP is programmed, its contents are automatically checked and the result is printed.

③ Check the following items:
Check printing of the termination message.

④ Test termination
The test terminates automatically after printing the termination print.

109	E----- 109	F----- 109
Normal end print	Error print	SSP table full print (NOTE)

Note: In this SSP check, set the data for check in the empty area of SSP entry REG and erase the data for check after completion of check. Therefore, SSP setting before check is not cleared. If, therefore, there is no SSP entry REG remained for SSP check, F-print (SSP entry register full print) is performed to terminate the program without check.

[10] Drawer open sensor test

① Key operation
110~113 → CA/AT

② Functional description
The drawer indicated by the job number is opened to check the proper action.
Drawer opened: O indicated
Drawer closed: C indicated
110: Drawer-1: Option drawer
111: Drawer-2: Remote drawer
112: Drawer-3: Remote drawer
113: Drawer-4: Remote drawer

DOT DISPLAY : D R A W E R x y

x: 1~4
y: O= Drawer opened
C= Drawer closed

③ Check the following items:
a) Check opening of the specified drawer.
b) Check the display indication when the drawer is open and close.

④ Any key depression terminates the test with the termination print.

11X	X: 0~3
Test termination print	

[11] Display test-2

① Key operation
116 → CA/AT

② Functional description
The display CGs in CKDC4 are checked. The 256 CGs are grouped into 32 blocks and each 8 characters is displayed on the dot display.
The check start with CG code 00H - 07H, and the following blocks are sequentially displayed when any key is pressed.

DOT DISPLAY : x y : O O O O O O O O

O: CG display position
xy: The initial code of each block is displayed in hexadecimal (For example, A0, B8)

③ Check the following items.
1. Check that the display is normal.
2. Check that there is no blur, defects, and unevenness.

④ Test termination
To terminate the test, set the mode key to any mode other than SRV mode.

116
Test termination print

[12] SIO test-1

① Key operation
117 → CA/AT

② Functional description
The following two kinds of loopback tests are carried out using the special service tool (UKOG-6704RCZZ) to check the trans and receive data, ready, and not ready signals.
Test-1: Checks ER – DR, RS-CD and RR-CS
Test-2: Checks TXD – RXD

③ Check the following items:
Successful test results must be checked on the display and the termination message print.

④ Test termination

117	EX---- 117
Termination print	

X = 1: Non connect error
2: Verify error
3: Hardware error
4: P-OFF
5: Timer overflow error

[13] Standard RAM test

① Key operation
120 → CA/AT

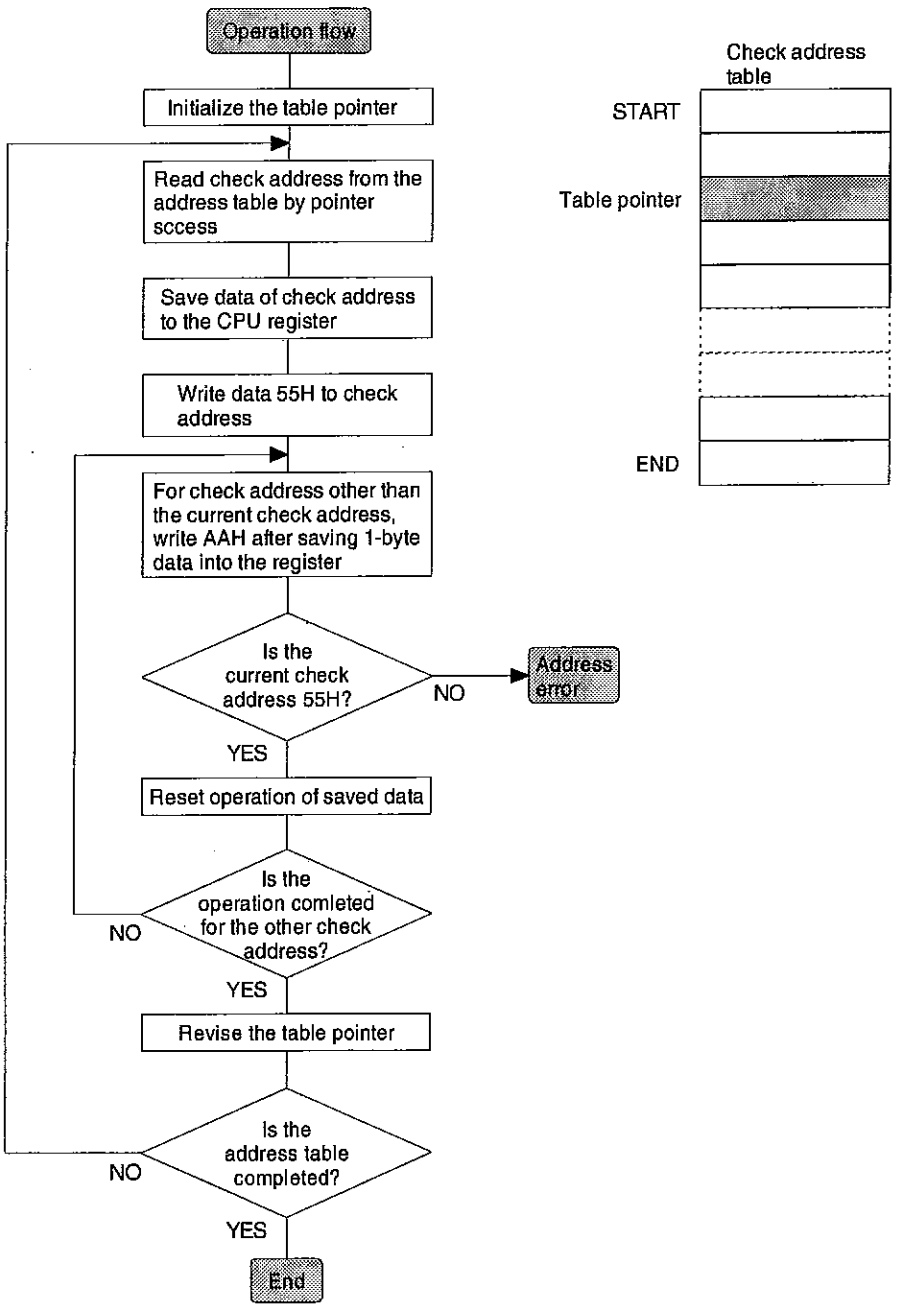
② Functional description
Perform the following check for the standard RAM 128 KByte SRAM. The memory contents should not be changed before and after the check.

Perform the following processes for memory address to be checked (1C0000H~1DFFFFH).
PASS1: Save memory data.

PASS2: Write data "0000H."
PASS3: Read and compare data "00H," write data "55H."
PASS4: Read and compare data "55H," write data "AAH."
PASS5: Read and compare data "AAH."
PASS6: Restore the memory data.

If a comtare error occurs in the check sequence PASS1-PASS6, an error print is made. If no error occurs through all address, the check ends normally.

The following address check is performed further.
Check point address = 1C0000H, 1C0001H
1C0002H, 1C0004H
1C0008H, 1C0010H
1C0020H, 1C0040H
1C0080H, 1C0100H
1C0200H, 1C0400H
1C0800H, 1C1000H
1C2000H, 1C4000H
1C8000H, 1D0000H



③ Check the following items:
Check the termination printout.

④ Test termination
The test terminates after printing the termination printout.
Termination printout:

Normal termination		120
Abnormal termination	Ex-----	120
		※※※※※

X = 1: Data check error
2: Address check error

Note: When an error occurs, the error print is performed and the check is terminated. The error occurrence address is shown in hexadecimal at positions shown with ※※※※※.

[14] Standard ROM test

① Key operation
130 → CA/AT

② Functional description
Sum check of the standard ROM (C00000H - C7FFFFH) is performed. If the lower two digits of SUM is 10H, it is normal.

DOT DISPLAY : S T D R O M

③ Check the following items:
Check the printout after the test.

④ Test termination
The test automatically terminates with termination message.

Normal termination print		130	Note
	S-ROM	27040※※※※※	
		※※※※※	
Error termination print	E-----	130	
	S-ROM	27040※※※※※	
		※※※※※	

Note: "※※※※※" means the ROM version number.
The underlined section (10 bytes) of code table is provided in the ROM as a standard and the table content is always printed.
The table position is the upper 10 digits of the ROM address.
The check sum correction address is the last address -0FH.

Note: In the case of the ER-ROM, the ROM version number is displayed in the upper and the lower stages.
In the case of the MASK-ROM (future specification), the MASK ROM code is displayed in the upper stage, and the ROM version number is displayed in the lower stage.

	130
S-ROM	27040RAL1A
	RAL1A
	400
O-ROM	27020RAP1A
	RAP1A

[15] R/J printer dot pulse width adjustment

The dot pulse width adjust circuit is provided to control the width of the current applied to the dot head of the printer KI-OB6754RC01, according to a supply voltage fluctuation.
When the circuit is changed with a new one for such as a repair work, the dot pulse width needs to be adjusted using the 200K pot VR1.

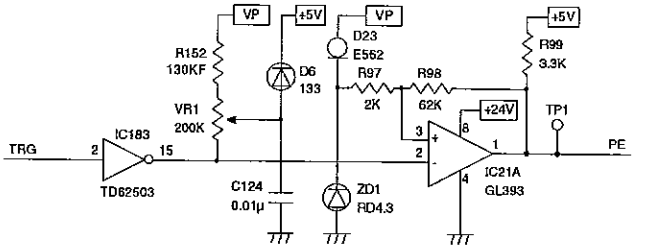


Fig. 3-3

Dot pulse adjusting method

1. Turn power on.
2. Measure the voltage of the VP line between the fuse F1 and GND. Use a digital voltmeter capable of measuring 100mV steps.
3. Set the MODE switch to the SRV position and start the diagnostic program Job #150 with the next command procedure.
   150 → CA/AT
4. Adjust pulse width of TPW at the test point TP1 as shown in the graph in Fig.3. The pulse width of TPW can be adjusted using the 200K pot VR1.
5. To terminate the diagnostic program, just press any key.

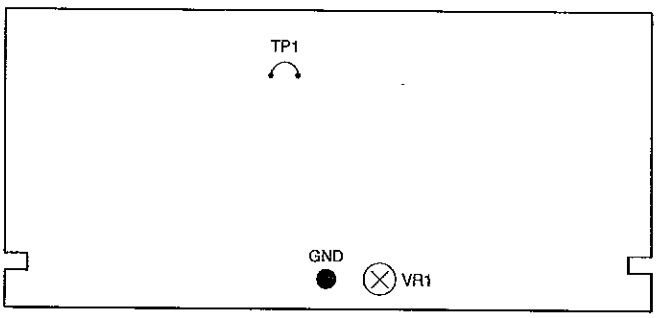
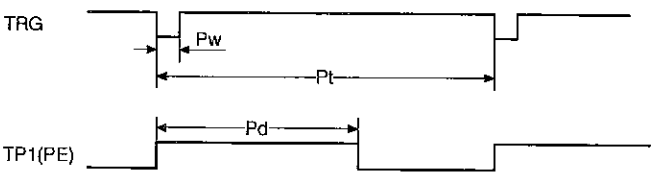


Fig. 3-4



Pw ≒ 4μsec
Pt ≧ 1000μsec
Pd is adjusted to 518 usec when Vp is +24.0V.

Fig. 3-5

* For the adjustment of VP, refer to CHAPTER 7. SERVICE PRECAUTION. (Printer printing speed adjustment)

[16] Option RAM test

① Key operation
20X → CA/AT

JOB #NO.	RAM NO.	Memory to be checked	Address area to be checked
200	Option RAM (main)	ER-01RA	1E0000H ≀ 1E7FFFH
201	Option RAM (main)	ER-02RA	1E0000H ≀ 1FFFFFH
202	ER-01MB RAM1	ER-02RA+ER-01MB	1E0000H ≀ 21FFFFH
203	ER-01MB RAM2	ER-02RA+ (ER-01MB+ER-02RA)	1E0000H ≀ 23FFFFH
204	ER-01MB RAM3	ER-02RA+ (ER-01MB+ER-02RAX2)	1E0000H ≀ 25FFFFH
205	ER-01MB RAM4	ER-02RA+ (ER-01MB+ER-02RAX3)	1E0000H ≀ 27FFFFH
206	ER-02MB	ER-02RA+ER-02MB	1E0000H ≀ 2FFFFFH

② Content
The following check are performed for the optional RAM.
The following process is performed for memory address to be checked.

PASS1: memory data save
PASS2: Data "00H" write
PASS3: Data "00H" read and comparison, data "55H" write
PASS4: Data "55H" read and comparison, data "AAH" write
PASS5: Data "AAH" read and comparison
PASS6: Memory data restore

If a compare error is found in the check sequence from PASS1 to PASS6, error print (error code E1) is performed. If there is no error found to the end of the last address, the operation is completed normally.

Then the following address check is performed by judging the option chip to be integrated. The check point addresses are as follows:

Check Address	JOB200	JOB201	JOB202	JOB203	JOB204	JOB205	JOB206
1E0000H	O	O	O	O	O	O	O
1E0001H	O	O	O	O	O	O	O
1E0002H	O	O	O	O	O	O	O
1E0004H	O	O	O	O	O	O	O
1E0008H	O	O	O	O	O	O	O
1E0010H	O	O	O	O	O	O	O
1E0020H	O	O	O	O	O	O	O
1E0040H	O	O	O	O	O	O	O
1E0080H	O	O	O	O	O	O	O
1E0100H	O	O	O	O	O	O	O
1E0200H	O	O	O	O	O	O	O
1E0400H	O	O	O	O	O	O	O
1E0800H	O	O	O	O	O	O	O
1E1000H	O	O	O	O	O	O	O
1E2000H	O	O	O	O	O	O	O
1E4000H	O	O	O	O	O	O	O
1E8000H	—	O	O	O	O	O	O
1F0000H	—	O	O	O	O	O	O
200000H	—	—	O	O	O	O	O
210000H	—	—	O	O	O	O	O
220000H	—	—	—	O	O	O	O
240000H	—	—	—	—	O	O	O
260000H	—	—	—	—	—	O	O
280000H	—	—	—	—	—	—	O

"O" in the table shows that the check point address in the horizontal column is valid, and "—" shows it is invalid.
When any error occurs in this address check, error code E2 is printed.

③ Check the following items.
Check the termination print.

④ Test termination
The test terminates after printing the termination printout.

Termination print

Normal termination		20X
Abnormal termination	EY- - - -	20X
		※※※※※※

20X: JOB # (200~206)
Y: Error code

Note: When an error occurs error print is performed and the error address is displayed in position ※※※※※※ in hexadecimal.

[17] Option RAM address test

① Key operation
30X → [TL] (X: 0~6)

JOB #NO.	RAM NO.	Memory to be checked	Address area to be checked
300	Option RAM (main)	ER-01RA	1E0000H ≀ 1E7FFFH
301	Option RAM (main)	ER-02RA	1E0000H ≀ 1FFFFFH
302	ER-01MB RAM1	ER-02RA+ER-01MB	1E0000H ≀ 21FFFFH
303	ER-01MB RAM2	ER-02RA+ (ER-01MB+ER-02RA)	1E0000H ≀ 23FFFFH
304	ER-01MB RAM3	ER-02RA+ (ER-01MB+ER-02RA×2)	1E0000H ≀ 25FFFFH
305	ER-01MB RAM4	ER-02RA+ (ER-01MB+ER-02RA×3)	1E0000H ≀ 27FFFFH
306	ER-02MB	ER-02RA+ER-02MB	1E0000H ≀ 2FFFFFH

② Functional description
The following check are performed for the optional RAM. Do not change.

Check Address	JOB300	JOB301	JOB302	JOB303	JOB304	JOB305	JOB306
1E0000H	O	O	O	O	O	O	O
1E0001H	O	O	O	O	O	O	O
1E0002H	O	O	O	O	O	O	O
1E0004H	O	O	O	O	O	O	O
1E0008H	O	O	O	O	O	O	O
1E0010H	O	O	O	O	O	O	O
1E0020H	O	O	O	O	O	O	O
1E0040H	O	O	O	O	O	O	O
1E0080H	O	O	O	O	O	O	O
1E0100H	O	O	O	O	O	O	O
1E0200H	O	O	O	O	O	O	O
1E0400H	O	O	O	O	O	O	O
1E0800H	O	O	O	O	O	O	O
1E1000H	O	O	O	O	O	O	O
1E2000H	O	O	O	O	O	O	O
1E4000H	O	O	O	O	O	O	O
1E8000H	—	O	O	O	O	O	O
1F0000H	—	O	O	O	O	O	O
200000H	—	—	O	O	O	O	O
210000H	—	—	O	O	O	O	O
220000H	—	—	—	O	O	O	O
240000H	—	—	—	—	O	O	O
260000H	—	—	—	—	—	O	O
280000H	—	—	—	—	—	—	O

"O" in the table shows that the check point address is valid, and "—" shows that it is invalid.

③ Check the following items.
Check the termination print.

④ Test termination
The test terminates after printing the termination printout.

Termination printout

Normal termination		30X
Abnormal termination	EY– – – –	30X
		※※※※※※

30X: JOB# (300~306)
Y: Error code

Note: When an error occurs error print is performed and the error address is displayed in position ※※※※※※ in hexadecimal.

[18] Option ROM test

① Key operation:
400 → [CA/AT]

② Functional description:
A sum check is done for the option ROM (Address hex C80000H thru CBFFFFH.)

DOT DISPLAY : O P T R O M

③ Check the following items:
Check the termination printout.

④ Test termination:
The test terminates after printing the termination printout.
Termination printout

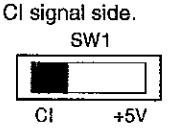
Normal termination		400
	O-ROM	27020※※※※※
		※※※※※
	E– – – – –	400
	O-ROM	27020※※※※※
		※※※※※

The underlined section must be the same as the standard ROM test specification. (Refer to JOB #130.)

[19] RS-232 test

The channel check of the scanner I/F RS-232 connector (D-sub, 9 pin) is performed.
Execute the following procedures with the power switch OFF.

- Set the I/F SW1 to the CI signal side.



- Connect the RS-232 loop back connector (UKOG–6705RCZZ).

1) Channel check

① Activation
The program is activated by JOB#500
SRV mode: 500 → [CA/AT]

② Contents to be tested
Information about connected RS-232 channel is printed.

* For RS-232 for the ER-A610 scanner, CH1 is used.

Printing digit

21	20	19	18	17	16	15	3	2	1
1	1	1	1	1	1	0	5	0	0
CH7	CH6	CH5	CH4	CH3	CH2	CH1			

CHn = 0 : Presence of channel
1 : Ansence of channel

③ Confirmed content
Printed contents and the setting of channel changeover switch on PWB are compared and confirmed.

④ Release
The program is terminated after the above contents are printed.

2) RS-232 Channel 1 check

① Activation
The program is activated by JOB#501.
SRV mode: 501 → [CA/AT] : Channel 1

② Contents to be tested
If the channel specified by JOB#CODE is not set, the machine performs the mis-operation processing. When the channel is set, the machine conducts the loop check concerning the channel specified by JOB#CODE by using the loopback connector.

The following three items are checked:

① Control signal check

② Data transfer check

③ Timer check (RS-232 onboard timer)

Check ① Control signal check ($\overline{ERn}$-$\overline{DRn}$•$\overline{CIn}$, $\overline{RSn}$-$\overline{CDn}$•$\overline{CSn}$ loop check)

OUTPUT		INPUT			
$\overline{ERn}$	$\overline{RSn}$	$\overline{DRn}$	$\overline{CIn}$	$\overline{CDn}$	$\overline{CSn}$
OFF	OFF	OFF	OFF	OFF	OFF
OFF	ON	OFF	OFF	ON	ON
ON	OFF	ON	ON	OFF	OFF
ON	ON	ON	ON	ON	ON

The read check about the above INPUT items and interrupt check of $\overline{CS}$, $\overline{CI}$ and $\overline{CD}$ are performed.

Read check: $\overline{ER}$ and $\overline{RS}$ are switched over in the order as shown in the above table to confirm the logic of $\overline{DR}$, $\overline{CI}$, $\overline{CD}$ and $\overline{CS}$.If the read logic is different from the one in the table, error print-outs occur.

Interrupt check: Allows the interruption of either of $\overline{CS}$, $\overline{CI}$ and $\overline{CD}$ one by one. (The mask is released.)
The interruption does not take place when each signal is turned on. Or if the interruption occurs when a signal is turned off, error print-outs occur.

Each of the above checks should be made in four cycles.

Note) $\overline{ERn}$ control selector jumper switch on the I/F board must be switched to the software control side.

Check ② Data transfer check (SDn-RDn loop check)
In this check, transfer 256-byte loopback data of $00 ~ $FF.

Note) The above check should be made with the baud rate set at 9600BPS.

Check ③ Timer check
Before making check ②, set the corresponding timer at 10ms for RCVDT activation, and check to see that:
1) $\overline{TRQ1}$ is not generated during the execution of check ②.
2) $\overline{TRQ1}$ is generated in 10msec. after check ② is finished.

③ Contents to be checked
If an error occurs during the above checks, following error print-outs occur. Even if an error occurs during check ①, the test is continued after the corresponding error print-out has occurred, but if an error occurs during the execution of check ② or ③, the test is terminated after the corresponding error print-out has occurred.
Note that when check ①, ② or ③ terminates, the termination print-out occurs irrespective of any errors that have occurred during the check. (The program terminates normally only when no error print-out has occurred.)

ERROR	ERROR PRINT	Contents
1	E1-ER DR	$\overline{ERn}$-$\overline{DRn}$ ERR
2	E2-ER CI	$\overline{ERn}$-$\overline{CIn}$ ERR
3	E3-RS CD	$\overline{RSn}$-$\overline{CDn}$ ERR
4	E4-RS CS	$\overline{RSn}$-$\overline{CSn}$ ERR
5	E5-CI INT	Interruption error of $\overline{CIn}$
6	E6-CD INT	Interruption error of $\overline{CDn}$
7	E7-CS INT	Interruption error of $\overline{CSn}$
8	E8-TXEMP	TXEMPn error
9	E9-TXEMP I	Interruption error of TXEMPn
10	E10-TXRDY	TXRDYn error
11	E11-TXRDY I	Interruption error of TXRDYn
12	E12-RCVRDY	RCVRDYn error (Reception is impossible. TRQ1 has occurred during execution of check ②.)
13	E13-RCVRDY I	Interruption error of RCVRDY
14	E14-SD RD	SDn-RDn ERR (Data error)
15	E15-SD RD	SDn-RDn ERR (Data error, Flaming error)
16	E16-TIMER	TIMERn error ($\overline{TMRQn}$ cannot be set after termination of check ②.)
17	E17-TIMER I	Interruption error of TRQ1

Errors that may occur during check ① (control signal check): E1 ~ E7
Errors that may occur during check ② (data transfer check): E8 ~ E15
Errors that may occur during check ③ (timer check): E12, E16 and E17

④ Cancellation
The program automatically terminates when a check is finished.

Termination print-out:

501

CHAPTER 6. DOWN LOAD FUNCTION

1. General

RAM data can be transmitted in the following two methods.
Save the data before servicing as follows:

① ECR ⟷ ECR

- Cable: ER-A5CB

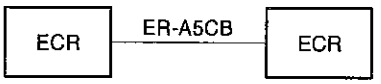


Fig. 1-1

② ECR ⟷ ER-02FD

- Cable: Cable (QCNW-7578RCZZ) packed with the ER-02FD

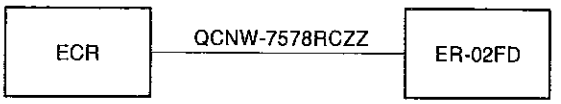


Fig. 1-2

2. SIO interface specification

1) Operation:	Simplex
2) Line configuration:	Direct connect
3) Data rate:	19200, 9600, 4800, 2400, 1200, 600, 300BPS (Selected by SRV JOB#903-A)
4) Sync mode:	Asynchronous
5) Checking:	Vertical parity (odd)
6) Code:	7 bits (ASCII)
7) Bit sequence:	LSB first
8) Line level:	TTL level
9) Data forma:	

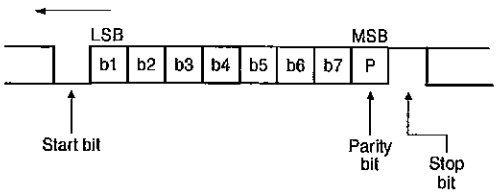


Fig. 2-1

3. Location of connector pins

① ER-A5CB

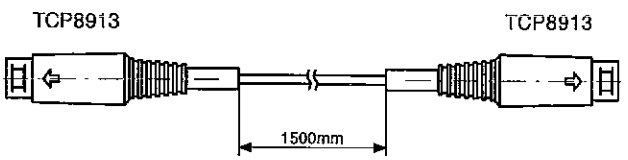


Fig. 3-1

Signal name	Pin No.
GND	1
$\overline{ER}$	2
$\overline{CD}$	3
$\overline{RR}$	4
$\overline{CS}$	5
$\overline{DR}$	6
RXD	7
TXD	8
$\overline{RS}$	9

Pin No.	Signal name
1	GND
2	$\overline{ER}$
3	$\overline{DR}$
4	RXD
5	TXD
6	$\overline{CD}$
7	$\overline{RR}$
8	$\overline{CS}$
9	$\overline{RS}$

Fig. 3-2

② QCNW-7578RCZZ

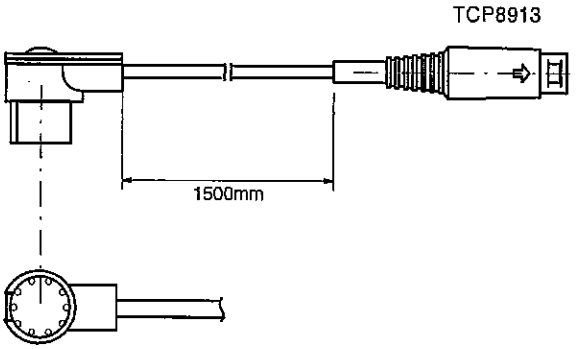


Fig. 3-3

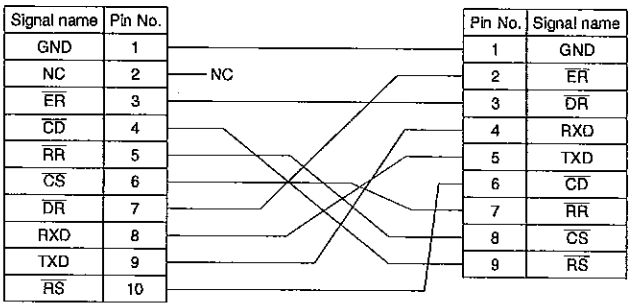


Fig. 3-4

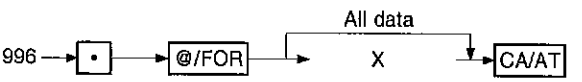
Interfacing signals

Pin No.	Signal name	In/Out	On level	Description
1	GND	—	—	Signal ground
2	$\overline{ER}$	Out	Low	Equipment ready
3	$\overline{DR}$	In	Low	Data set ready
4	RXD	In	High: MARK Low: SPACE	Receive data
5	TXD	Out	High: MARK Low: SPACE	Transmit data
6	$\overline{CD}$	In	Low	Carrier detect
7	$\overline{RR}$	Out	Low	Ready to receive
8	$\overline{CS}$	In	Low	Clear to send
9	$\overline{RS}$	Out	Low	Request to send

4. Application specification

The following service (SRV) modes are available for the serial data transfer of the ER-A610.

1) Data transmit (Source side)
X: 0=SSP DATA

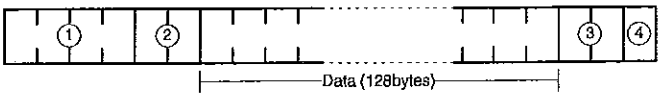


1 = Standard RAM+01RA/02RA
2 = 01MB (0.5MB)/02MB (0.5MB:1st half)
3 = 02MB (0.5MB: 2nd half)

2) Data receive (Target)

5. Data format

A single byte image of the RAM data to be transmitted is divided into a high order 4 bits and low order 4 bits and converted into ASCII code. Then, the image of the memory is sent in the following format:



① Memory top address: 0000H ~ FFFFH
Top address of the memory to be transmitted in ASCII number.

② Page:1D ~ 1F
Page of the memory to be transmitted in ASCII number.

③ Sum check

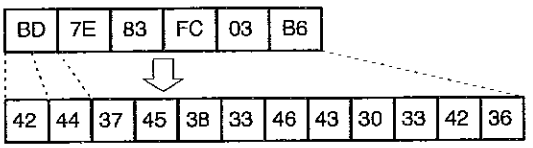
④ End code:
Hex 0D

NOTE:

- In order that contents of RAM memory may not over-ride pages for this job, RAM image is sent in unit of 64 bytes from the address 0000. In other words, 128 bytes are sent at one time on the transmit data format.

RAM DATA FORMAT

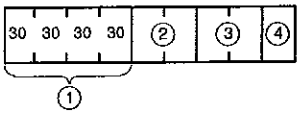
Exhibit:



Code table

HEX	ASCII	Character
0	30	0
1	31	1
2	32	2
3	33	3
4	34	4
5	35	5
6	36	6
7	37	7
8	38	8
9	39	9
A	41	A
B	42	B
C	43	C
D	44	D
E	45	E
F	46	F

6. END record



① End message:
Fixed to 30303030.

② End massage:
Fixed to 4646.

③ Sum check

④ End code:
CR (0D)

7. Operational method

1) To prepare an ER-A610 to receive data from another ER-A610 or the ER-02FD, the memory size of the receiving unit must the same as or greater than the sending unit.

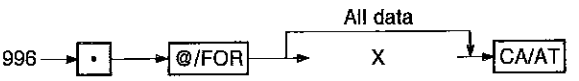
2) Master reset the receiving ER-A610.

3) Match the baud rate of the transmitter with the receiver using JOB#995 in the SRV mode.

4) Connect loader cable (QCNW-7578RCZZ or ER-A5CB) between ER-A610s.

5) Set the receiving ER-A610 ready to receive.

6) Start the sending ER-A650.



X: 0 = SSP
1 = Standard RAM+01RA/02RA
2 = 01MB (0.5MB)/02MB (0.5MB:1st half)
3 = 02MB (0.5MB: 2nd half)

7) Transmission status.
Description of error status
1: Application error (Command error)
2: Line error (DTR OFF)
3: Application error (Parity error)
4: Application error (Check sum error)
5: Application error (Data size error)
6: Hard ware error
7: Power off error
10: Time out error
11: Application error (Transmit data size error)
12: Application error (Block sequence error)
13: Memory full error

8) Service reset the receiving ER-A610.

8. Saving/Loading of data to/From the FD unit Configuration

1) Turn off the power switch of the ER-02FD, and set the DIP switches of the FD unit as follows:

ER-02FD (The ER-01FD functions of the ER-02FD are used.)

DS-1								DS-2			
1	2	3	4	5	6	7	8	1	2	3	4
OFF	ON	OFF	ON	ON	OFF	OFF	OFF	X	OFF	OFF	OFF

Data rate

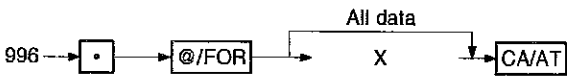
4	6	Rate [bps]
OFF	OFF	19200
ON	OFF	9600
OFF	ON	4800
ON	ON	2400

Disk format
CCP/M: OFF
PC-DOS: ON

2) Connect the QCNW-7578RCZZ cable.

Saving data

1) Turn on the power switch and insert a floppy disk which has been formatted.
2) Start the SEND JOB on the ECR side as follows:



X: 0 = SSP
1 = Standard RAM+01RA/02RA
2 = 01MB (0.5MB)/02MB (0.5MB:1st half)
3 = 02MB (0.5MB: 2nd half)

3) Data transmission is started and the green lamp on the ER-02FD blinks.

Loading data

1) Turn on the power switch and insert the floppy disk which stores the data.
2) Start the RECEIVE JOB on the ECR side as follows:

3) Press the [SEND] key on the FD unit.
4) Data transmission is started and the Green lamp on the ER-02FD blinks.
5) Service reset the ECR.

CHAPTER 7. SERVICE PRECAUTION

1. Hints and tips when installing the RAM chip option (ER-02RA)

1) When the RAM option (ER-02RA) is to be installed to the main PWB, be sure that the ER-02RA is facing in the right direction.

2. Printer motor lock

In the ER-A610, the motor will automatically turn off when a premature halting of the timing signals occurs due to a paper misfeed, ribbon jam, intrusion of alien object, etc. When the motor stops, an intermittent beeping will occur, with no indication in the display.

<How to reset the motor lock>: R/J printer

1) Disconnect the AC cord from the wall outlet. And remove the cause.
2) When power is restored, the following is displayed.

PRINTER ERROR

Fig. 2-1

3) Depress the [CL] key to return the ER-A650 to the point where the cause happened. The power failure symbols will be printed after a line feed.
4) Print sample

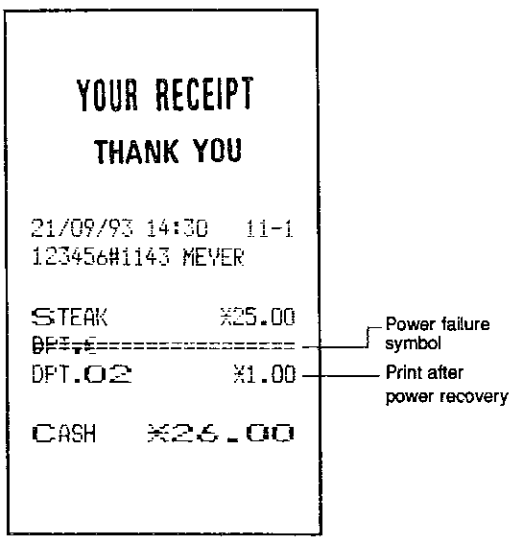


Fig. 2-2

3. Note for upper cabinet installation

When installing the upper cabinet again, be sure to connect the GND wire (QCNW-7120RCZZ) to the proper connector in front of the printer.

4. Others

1) If D1 shorts, the VRAM is shorted with the 5V supply.
In this event, normal operation is usually possible, except that it may not recharge the battery, failing to back it up, resulting in memory frustration.

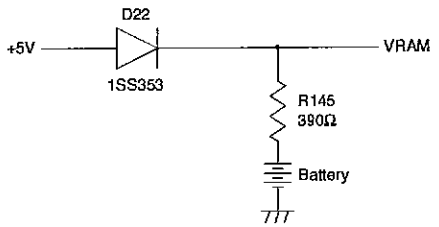


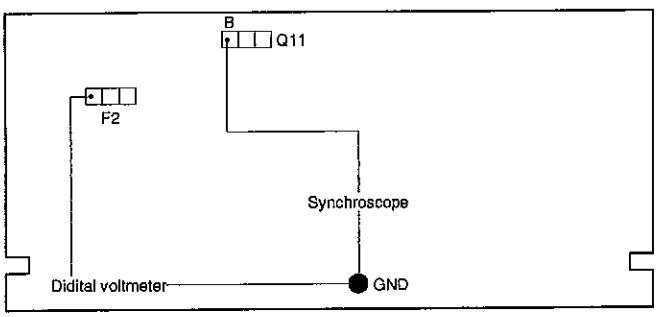
Fig. 4-1

2) When installing the option I/F PWB, be sure to connect it to the left side (under the power PWB) when viewed from the rear of the body. Do not use the right side (under the printer).
3) When fuse F1 above the main PWB is blown off, be sure to check the zenor diode ZD2 (VHERD5.6FP3-1) and the thyristor Q2 (VHSDRA2TE//–1) for any damage as well as replace F1. If the diode is damaged, replace it with new one.
4) When removing or installing the option slot rear cover, be sure to lift up the pop-up display. Especially when installing the cover, be sure not to pinch the pop-up display cable between the upper cabinet and the cover.

5. Printer printing speed adjustment

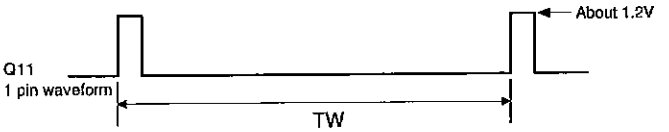
When the printer unit or the power PWB is replaced, the following adjustments should be performed.

1) Tools required for adjustment
   ① A synchroscope or a universal counter
   ② A digital voltmeter
2) Adjustment procedure
   ① Remove fuse F2 from the main PWB.
   ② Connect the probe of the synchroscope or the digital voltmeter with 1 pin and GND of Q11 (KTD1414) on the main PWB.
   ③ Connect the digital voltmeter pin with fuse F2 and GND of the main PWB.



   ④ Perform the master reset.
   ⑤ Turn VR1 on the PS PWB to adjust the voltage to 26.4V (Approx. 2.7 lines/sec).
   * Adjust VP so that it is in the range of 24V to 26.4V.
   ⑥ Perform the printing procedure. (Printing is not performed because the fuse is removed.)

   ⑦ Measure the time of TW with the waveform of Q11 1 pin as shown in the figure below.



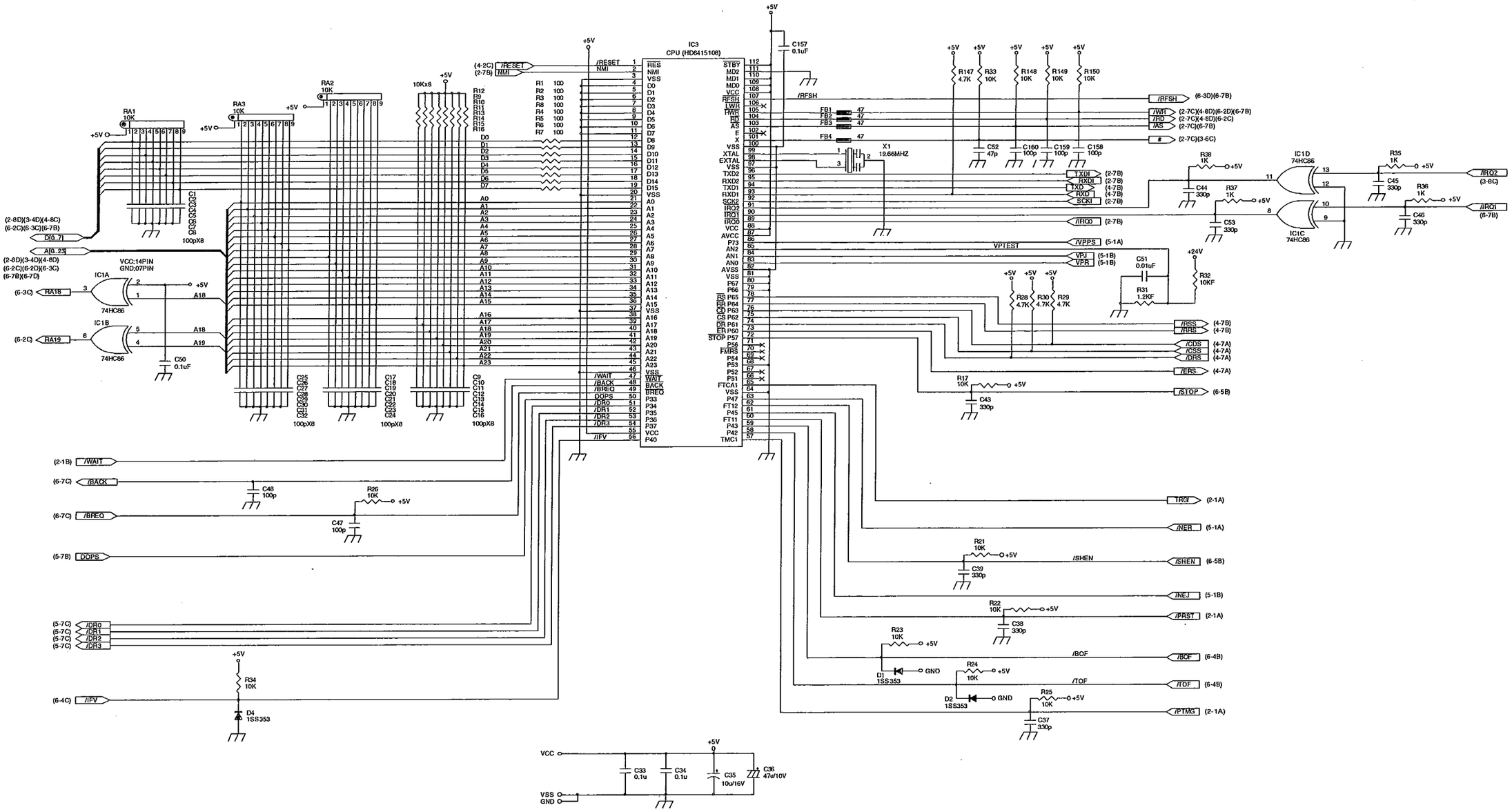
   ⑧ TW ≧ 357 ms: The adjustment is completed.
   TW < 357 ms: Adjust VR1 on the PS PWB so that TW may be 357 ms ±5 ms.
   ⑨ Turn off the power and disconnect the probe.
   ⑩ Attach the fuse to the original position.

6. For the adjustment of printer dot pulse, refer to CHAPTER 5. TEST FUNCTION, Test No. 150.

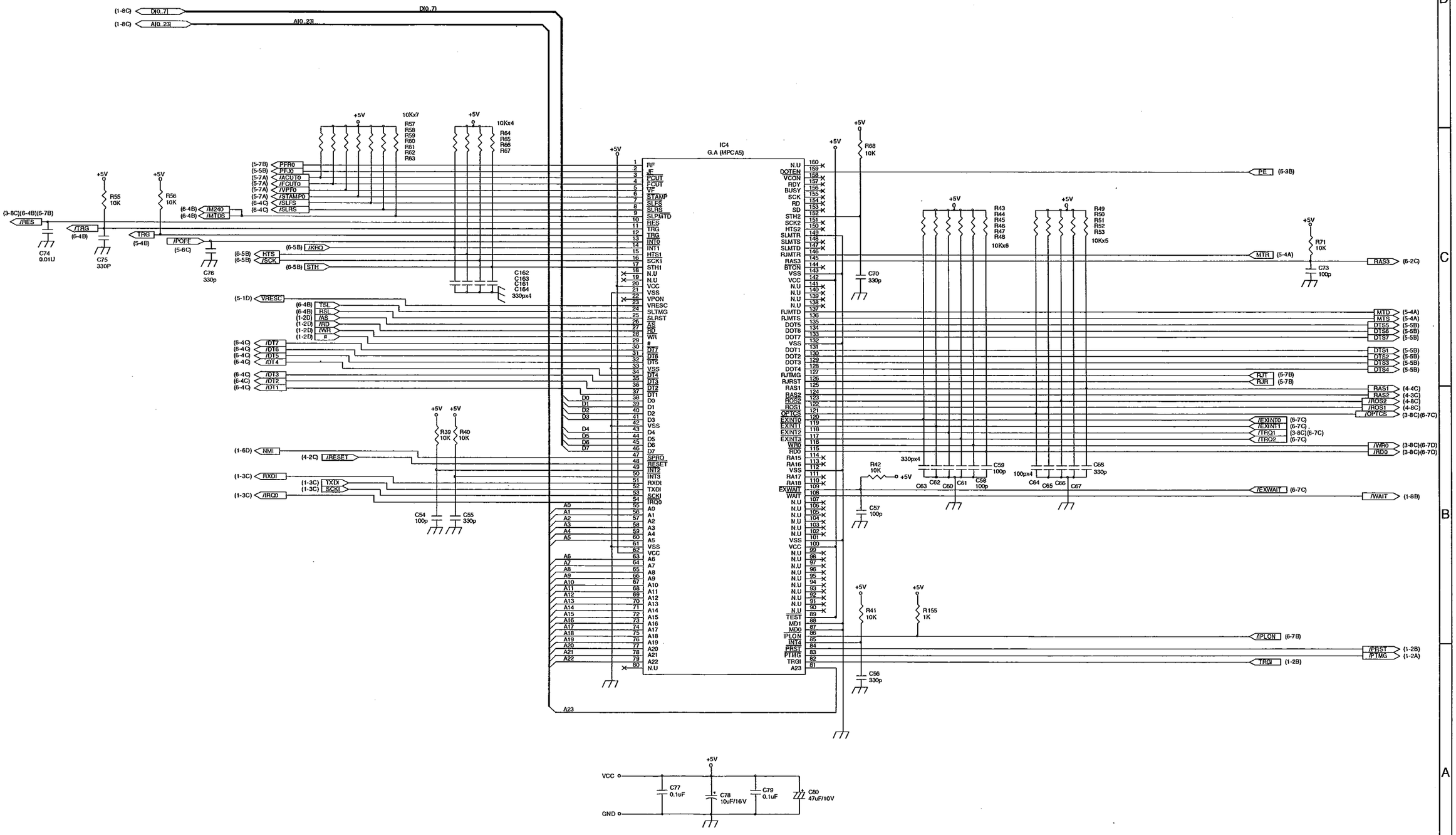
CHAPTER 8. CIRCUIT DIAGRAM & PWB LAYOUT

1. Main PWB circuit diagram

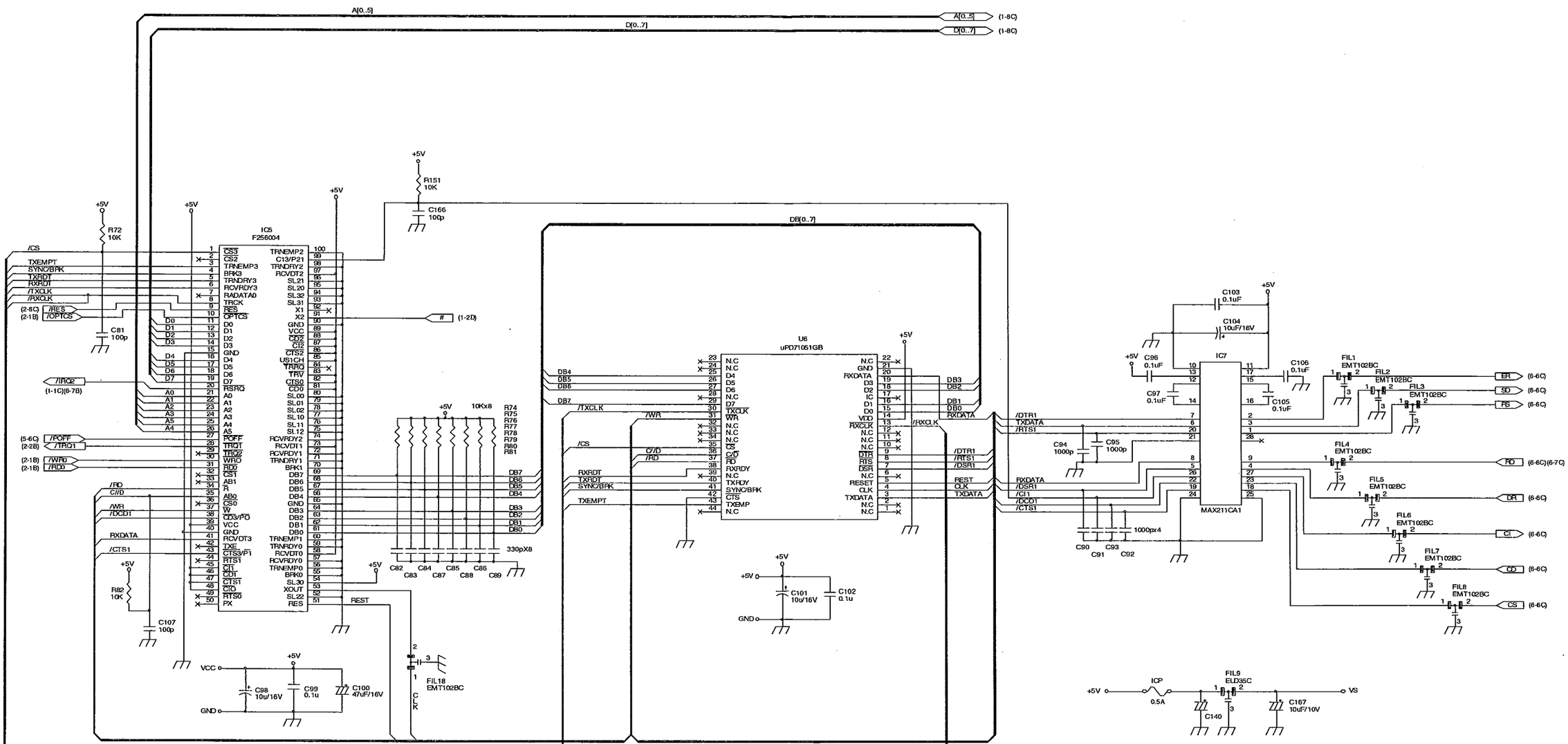
1/6

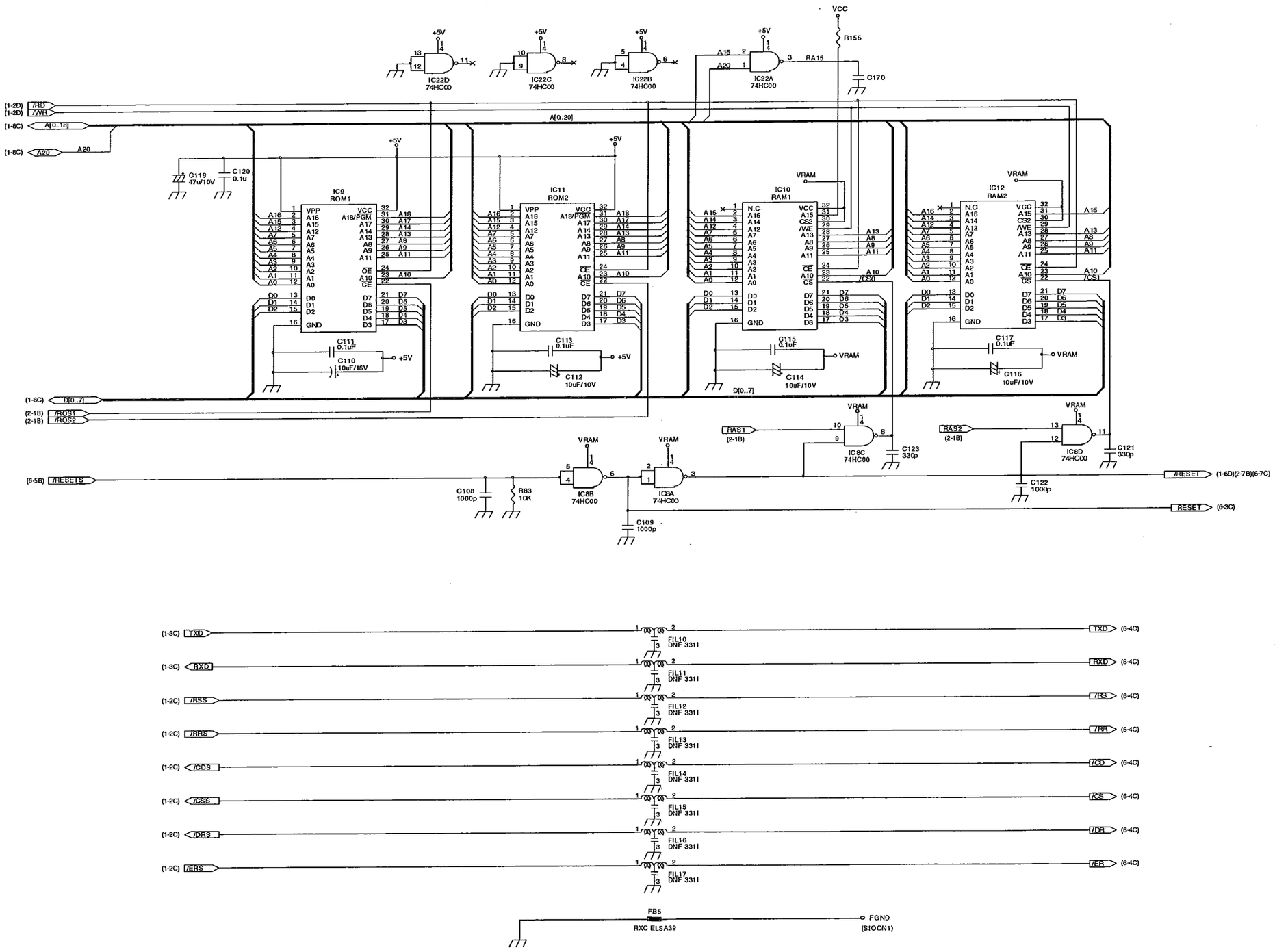


2/6

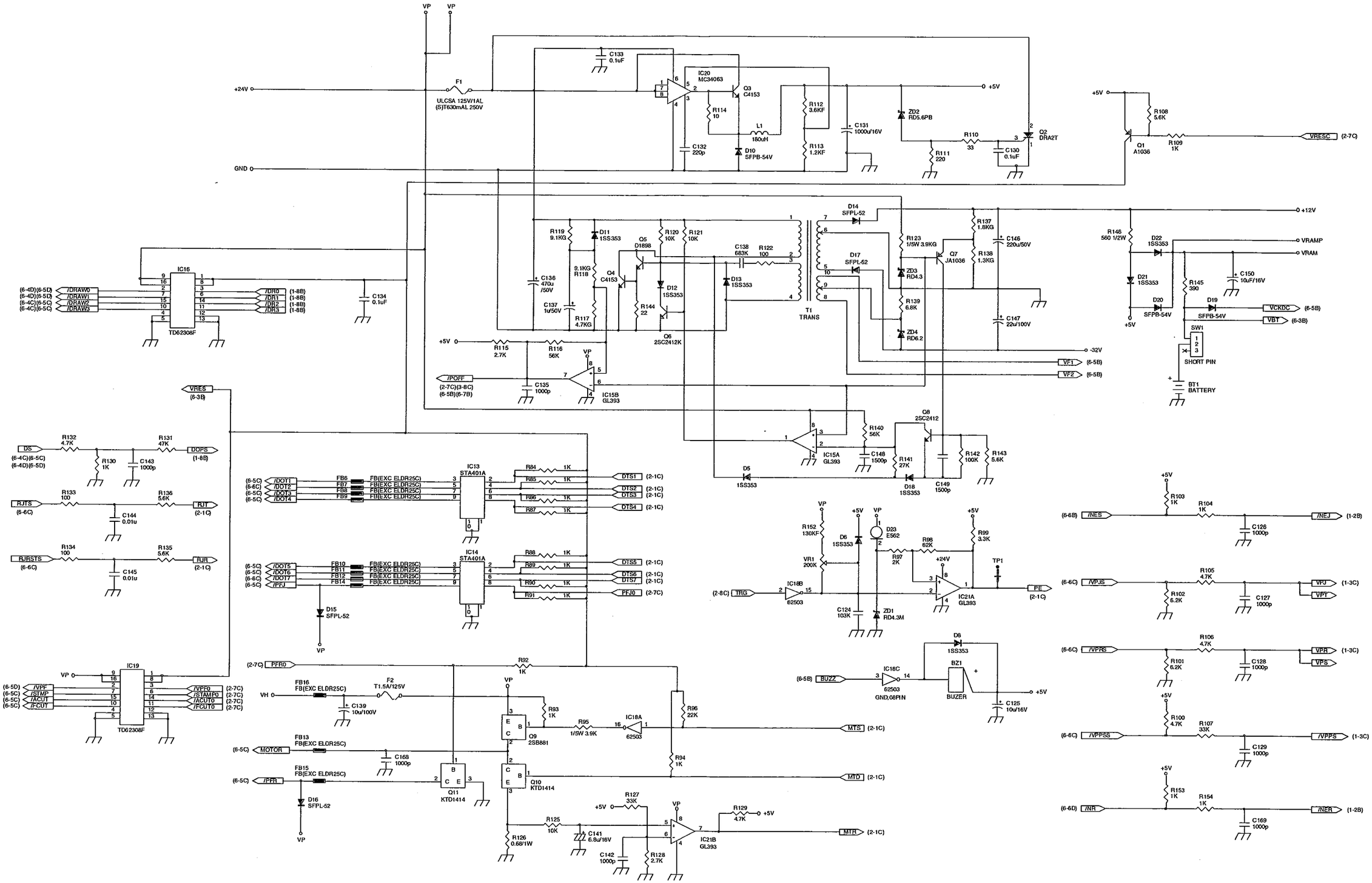

(1-8C) D[0..7]
D[0..7]
(1-8C) AI[0..23]
AI[0..23]
+5V
10Kx7
R57
R58
R59
R60
R61
R62
R63
10Kx4
R64
R65
R66
R67
(5-7B) PFR0
(5-5B) PFJ0
(5-7A) /ACUT0
(5-7A) /FCUT0
(5-7A) /VPF0
(5-7A) /STAMP0
(6-4C) /SLFS
(6-4C) /SLRS
(6-4B) /M240
(6-4B) /MTDS
R55 10K
R56 10K
(3-8C)(6-4B)(6-7B) /RES
/TRG (6-4B)
TRG (5-4B)
/POFF (5-6C)
C74 0.01U
C75 330P
C76 330p
(6-5B) /KRQ
(6-5B) HTS
(6-5B) /SCK
(6-5B) STH
C162
C163
C161
C164
330px4
(5-1D) VRESC
(6-4B) TSL
(6-4B) RSL
(1-2D) /AS
(1-2D) /RD
(1-2D) /WR
(1-2D) #
(6-4C) /DT7
(6-4C) /DT6
(6-4C) /DT5
(6-4C) /DT4
(6-4C) /DT3
(6-4C) /DT2
(6-4C) /DT1
+5V +5V
R39 10K
R40 10K
(1-6D) NMI
(4-2C) /RESET
(1-3C) RXDI
(1-3C) TXDI
(1-3C) SCKI
(1-3C) /IRQ0
C54 100p
C55 330p
IC4
G.A (MPCA5)
RF
IF
FCUT
FCUT
VF
STAMP
SLFS
SLRS
SLPMTD
RES
TRG
TRG
INT0
INT1
HTS1
SCK1
STH1
N.U
N.U
VCC
VSS
VPON
VRESC
SLTMG
SLRST
AS
RD
WR
#
DT7
DT6
DT5
VSS
DT4
DT3
DT2
DT1
DT0
D0
D1
D2
D3
VSS
D4
D5
D6
D7
SPRQ
RESET
INT2
INT3
RXDI
TXDI
SCKI
IRQ0
A0
A1
A2
A3
A4
A5
VSS
VCC
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
A19
A20
A21
A22
N.U
A23
N.U
DOTEN
VCON
RDY
BUSY
SCK
RD
SD
STH2
SCK2
HTS2
SLMTR
SLMTS
SLMTD
RJMTR
RAS3
BYON
VSS
VCC
N.U
N.U
N.U
N.U
N.U
VSS
RJMTD
RJMTS
DOT5
DOT6
DOT7
VSS
DOT1
DOT2
DOT3
DOT4
RJMTG
RJRST
RAS1
RAS2
ROSS
ROS1
OPTCS
EXINT0
EXINT1
EXINT2
EXINT3
WR0
RD0
RA15
RA16
VSS
RA17
RA18
EXWAIT
WAIT
N.U
N.U
N.U
N.U
N.U
VSS
VCC
N.U
N.U
N.U
N.U
N.U
N.U
N.U
N.U
N.U
TEST
MD1
MD0
IPLON
INT4
PRST
PTMG
TRGI
A23
+5V
R68 10K
C70 330p
PE (5-3B)
+5V
R43
R44
R45
R46
R47
R48
10Kx6
+5V
R49
R50
R51
R52
R53
10Kx5
MTR (5-4A)
+5V
R71 10K
C73 100p
RAS3 (6-2C)
MTD (5-4A)
MTS (5-4A)
DTS6 (5-5B)
DTS6 (5-5B)
DTS7 (5-5B)
DTS1 (5-5B)
DTS2 (5-5B)
DTS3 (5-5B)
DTS4 (5-5B)
RJT (5-7B)
RJR (5-7B)
RAS1 (4-4C)
RAS2 (4-3C)
/ROS2 (4-8C)
/ROS1 (4-8C)
/OPTCS (3-8C)(6-7C)
/EXINT0 (6-7C)
/EXINT1 (6-7C)
/TRG1 (3-8C)(6-7C)
/TRG2 (6-7C)
/WR0 (3-8C)(6-7D)
/RD0 (3-8C)(6-7D)
330px4
C59 100p
C62
C60
C61
C58 100p
100px4
C68 330p
C64
C65
C66
C67
R42 10K
+5V
C57 100p
/EXWAIT (6-7C)
/WAIT (1-8B)
+5V
R41 10K
+5V
R155 1K
C56 330p
/PLON (6-7B)
/PRST (1-2B)
/PTMG (1-2A)
TRGI (1-2B)
VCC
GND
C77 0.1uF
C78 10uF/16V
C79 0.1uF
C80 47uF/10V

3/6

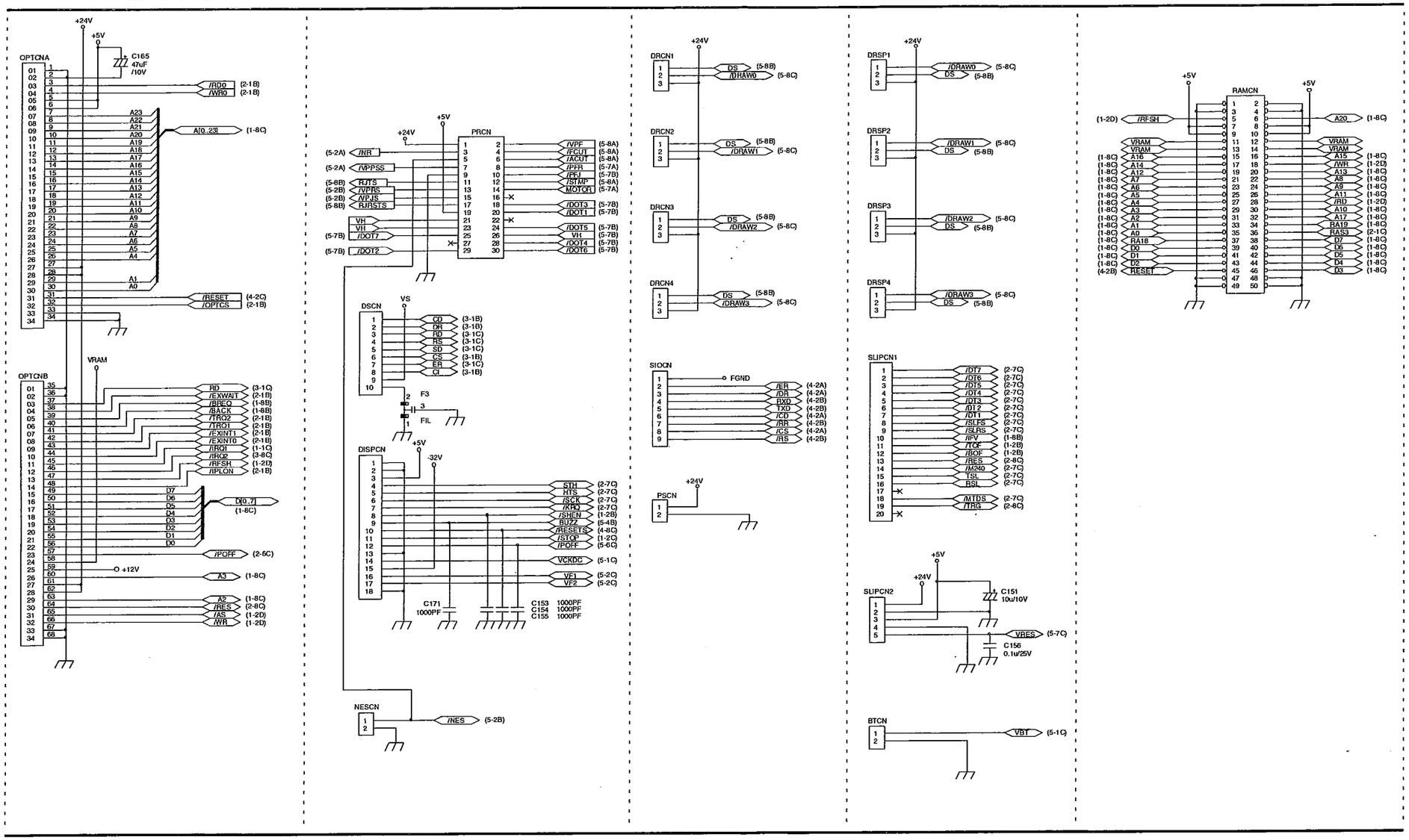

A[0..5]
D[0..7]
A[0..5] (1-8C)
D[0..7] (1-8C)
IC5
F256004
U6
uPD71051GB
MAX211CA1
IC7
DB[0..7]
/CS
TXEMPT
SYNC/BRK
TXRDT
RXRDT
/TXCLK
/RXCLK
/WR
/RD
C/D
RXDATA
/CTS1
/DTR1
/RTS1
/DSR1
/DCD1
/CI
REST
R72 10K
R151 10K
C166 100p
C81 100p
C107 100p
R82 10K
C82 C83 C84 C85 C86 C87 C88 C89
330pX8
10Kx8
R74 R75 R76 R77 R78 R79 R80 R81
C98 10u/16V
C99 0.1u
C100 47uF/16V
FIL18 EMT102BC
C101 10u/16V
C102 0.1u
C103 0.1uF
C104 10uF/16V
C96 0.1uF
C97 0.1uF
C106 0.1uF
C105 0.1uF
C94 1000p
C95 1000p
1000pX4
C90 C91 C93 C92
FIL1 EMT102BC
FIL2 EMT102BC
FIL3 EMT102BC
FIL4 EMT102BC
FIL5 EMT102BC
FIL6 EMT102BC
FIL7 EMT102BC
FIL8 EMT102BC
ER (6-6C)
SD (6-6C)
RS (6-6C)
RD (6-6C)(6-7C)
DR (6-6C)
CI (6-6C)
CD (6-6C)
CS (6-6C)
ICP
0.5A
FIL9 ELD35C
C140
C167 10uF/10V
VS
+5V
GND
VCC
(2-8C) /RES
(2-1B) /OPTCS
(1-1C)(6-7B) /IRQ2
(5-6C) /POFF
(2-2B) /TRQ1
(2-1B) /WR0
(2-1B) /RD0
(1-2D)
(1-1C)(6-7B)


IC22D 74HC00
IC22C 74HC00
IC22B 74HC00
IC22A 74HC00
+5V
VCC
R156
C170
A[0..20]
A20
C119 47u/10V
C120 0.1u
IC9 ROM1
IC11 ROM2
IC10 RAM1
IC12 RAM2
VRAM
C111 0.1uF
C110 10uF/16V
C113 0.1uF
C112 10uF/10V
C115 0.1uF
C114 10uF/10V
C117 0.1uF
C116 10uF/10V
D[0..7]
/RD
/WR
A[0..18]
/ROS1
/ROS2
/RESETS
RAS1
RAS2
IC8C 74HC00
IC8D 74HC00
C123 330p
C121 330p
C122 1000p
IC8B 74HC00
IC8A 74HC00
C108 1000p
R83 10K
C109 1000p
/RESET
RESET
/TXD
/RXD
/RRS
/RRR
/CDS
/CSS
/DRS
/ERS
FIL10 DNF 331I
FIL11 DNF 331I
FIL12 DNF 331I
FIL13 DNF 331I
FIL14 DNF 331I
FIL15 DNF 331I
FIL16 DNF 331I
FIL17 DNF 331I
FB5
RXC ELSA39
FGND
(SIOCN1)

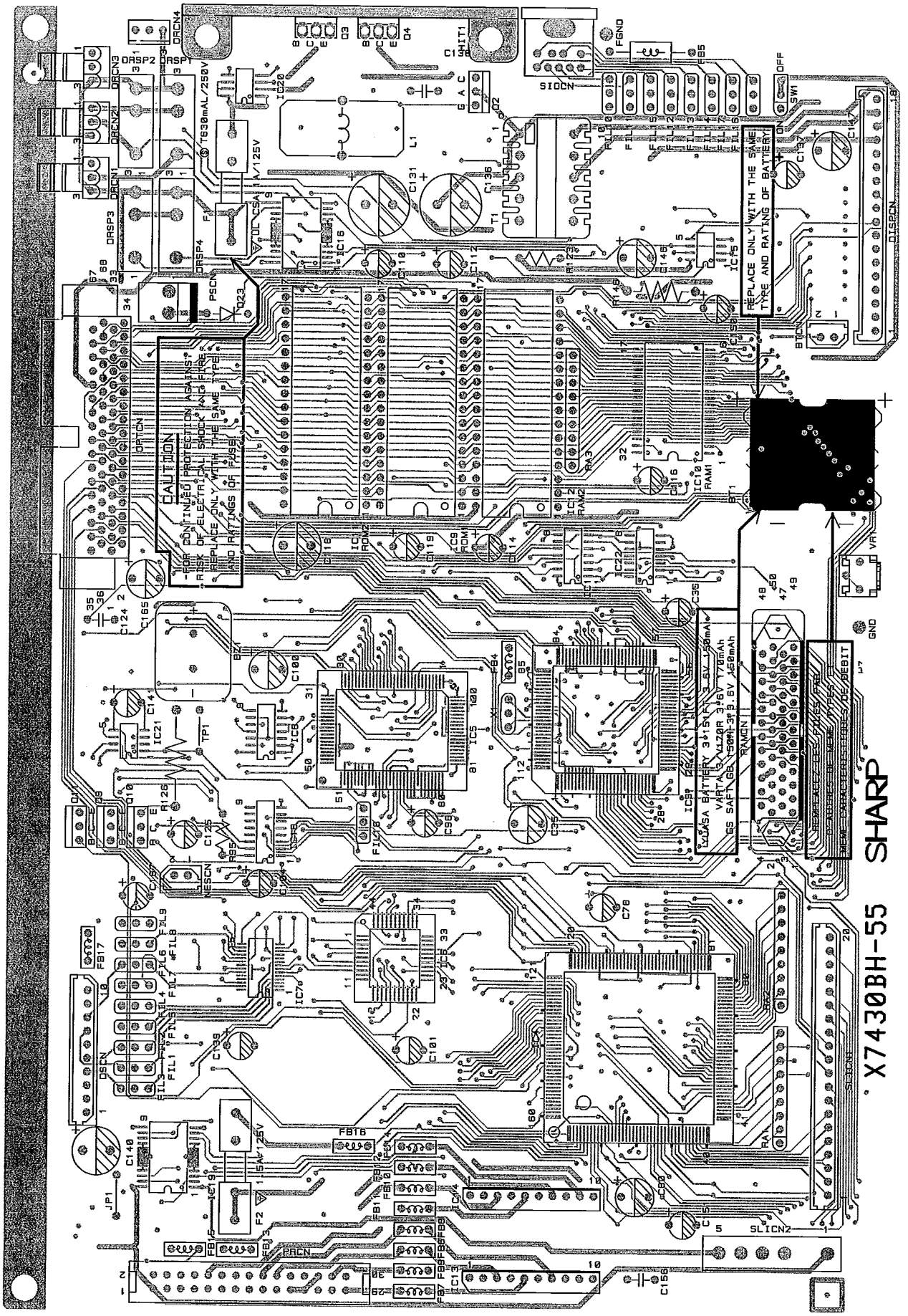
5/6


VP
+24V
F1
ULCSA 125V/1AL
(S)T630mAL 250V
GND
C133 0.1uF
IC20 MC34063
Q3 C4153
R114 10
L1 180uH
R112 3.6KF
R113 1.2KF
C131 1000u/16V
C132 220p
D10 SFPB-54V
ZD2 RD5.6PB
R110 33
R111 220
C130 0.1uF
Q2 DRA2T
+5V
R108 5.6K
Q1 A1036
R109 1K
VRESC (2-7C)
IC16
TD62308F
/DRAW0 /DRAW1 /DRAW2 /DRAW3
/DR0 /DR1 /DR2 /DR3 (1-8B)
C134 0.1uF
R119 9.1KG
D11 1SS353
Q5 D1898
R120 10K
R121 10K
C138 683K
R122 100
C136 470u /50V
9.1KG R118
Q4 C4153
C137 1u/50V
R117 4.7KG
R144 22
D12 1SS353
D13 1SS353
Q6 2SC2412K
TI TRANS
D14 SFPL-52
D17 SFPL-52
R123 1/5W 3.9KG
ZD3 RD4.3
R139 6.8K
ZD4 RD6.2
R137 1.8KG
R138 1.3KG
Q7 JA1036
C146 220u/50V
C147 22u/100V
+12V
R146 560 1/2W
D22 1SS353
D21 1SS353
D20 SFPB-54V
R145 390
C150 10uF/16V
D19 SFPB-54V
VRAMP
VRAM
VCKDC (6-5B)
VBT (6-3B)
SW1
SHORT PIN
BT1 BATTERY
-32V
VF1 (6-5B)
VF2 (6-5B)
R115 2.7K
R116 56K
/POFF
(2-7C)(3-8C)
(6-5B)(6-7B)
C135 1000p
IC15B GL393
VRES
(6-3B)
Q8 2SC2412
R140 56K
IC15A GL393
C148 1500p
R141 27K
D18 1SS353
C149 1500p
R142 100K
R143 5.6K
D5 1SS353
R132 4.7K
R131 47K
DS
(6-4C)(6-5C)
(6-4D)(6-5D)
DOPS (1-8B)
R130 1K
C143 1000p
R133 100
R136 5.6K
RJTS
(6-6C)
RJT (2-1C)
C144 0.01u
R134 100
R135 5.6K
RJRSTS
(6-6C)
RJR (2-1C)
C145 0.01u
IC13 STA401A
IC14 STA401A
/DOT1 /DOT2 /DOT3 /DOT4
/DOT5 /DOT6 /DOT7 /PFJ
FB6 FB7 FB8 FB9
FB10 FB11 FB12 FB14
FB(EXC ELDR25C)
R84 R85 R86 R87 R88 R89 R90 R91 1K
DTS1 DTS2 DTS3 DTS4 DTS5 DTS6 DTS7 (2-1C)
PFJ0 (2-7C)
D15 SFPL-52
VP
IC19
TD62308F
/VPF /STMP /ACUT /FCUT
/VPF0 /STAMP0 /ACUT0 /FCUT0 (2-7C)
PFR0 (2-7C)
R92 1K
FB16 FB(EXC ELDR25C)
F2 T1.5A/125V
VH
C139 10u/100V
R93 1K
R95 1/5W 3.9K
IC18A 62503
Q9 2SB881
R96 22K
MTS (2-1C)
FB13 FB(EXC ELDR25C)
MOTOR (6-5C)
C168 1000p
R94 1K
MTD (2-1C)
FB15 FB(EXC ELDR25C)
PFR (6-5C)
Q11 KTD1414
Q10 KTD1414
D16 SFPL-52
R125 10K
R126 0.68/1W
C141 6.8u/16V
C142 1000p
R127 33K
R128 2.7K
IC21B GL393
R129 4.7K
MTR (2-1C)
R152 130KF
D6 1SS353
D23 E562
VR1 200K
IC18B 62503
TRG (2-8C)
R97 2K
R98 62K
R99 3.3K
+24V
TP1
PE (2-1C)
IC21A GL393
C124 103K
ZD1 RD4.3M
D8 1SS353
IC18C 62503 GND,08PIN
BUZZ (6-5B)
BZ1 BUZZER
C125 10u/16V
/INES (6-6B)
R103 1K
R104 1K
C126 1000p
/INEJ (1-2B)
/VPJS (6-6C)
R105 4.7K
R102 6.2K
C127 1000p
VPJ (1-3C)
VPT
/VPRS (6-6C)
R106 4.7K
R101 6.2K
C128 1000p
VPR (1-3C)
VPS
/VPPSS (6-6C)
R100 4.7K
R107 33K
C129 1000p
/VPPS (1-3C)
/INR (6-6D)
R153 1K
R154 1K
C169 1000p
/INER (1-2B)

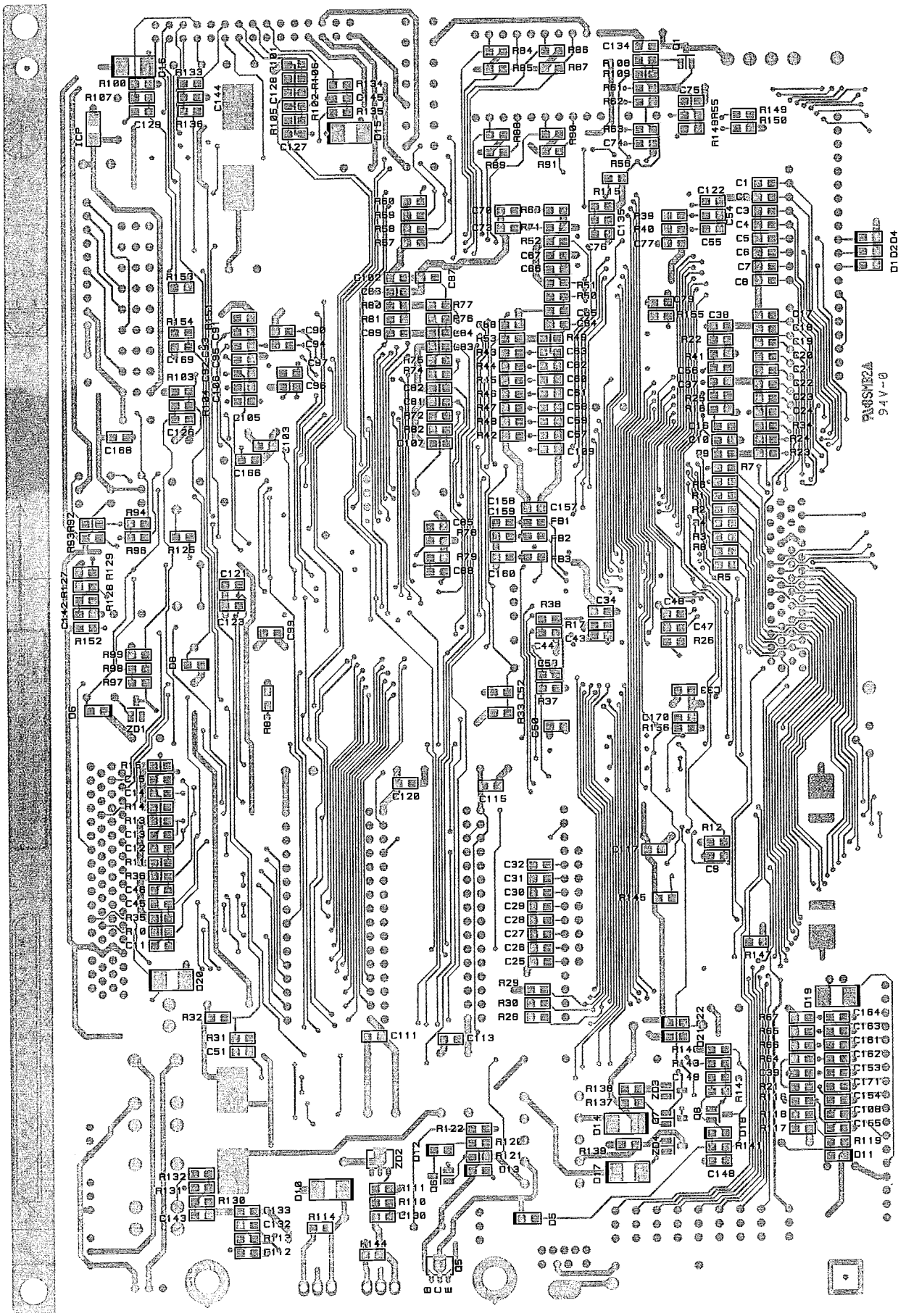
2.MAIN PWB CONECTOR TABLE



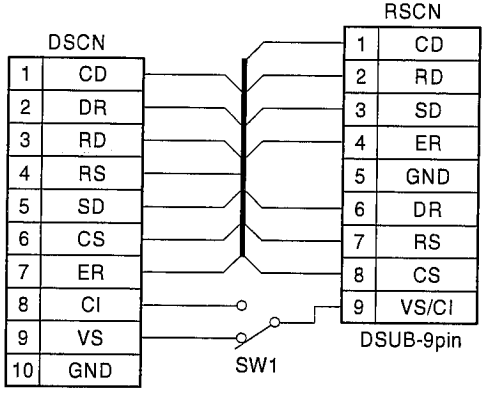
2. Main PWB layout (Parts side)



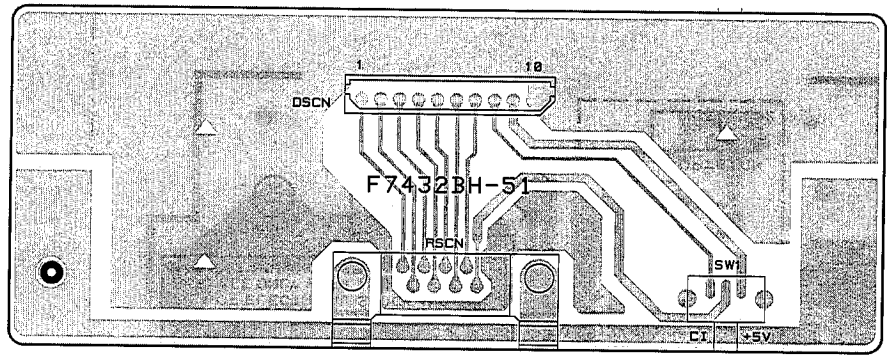
3. Main PWB layout (Solder side)



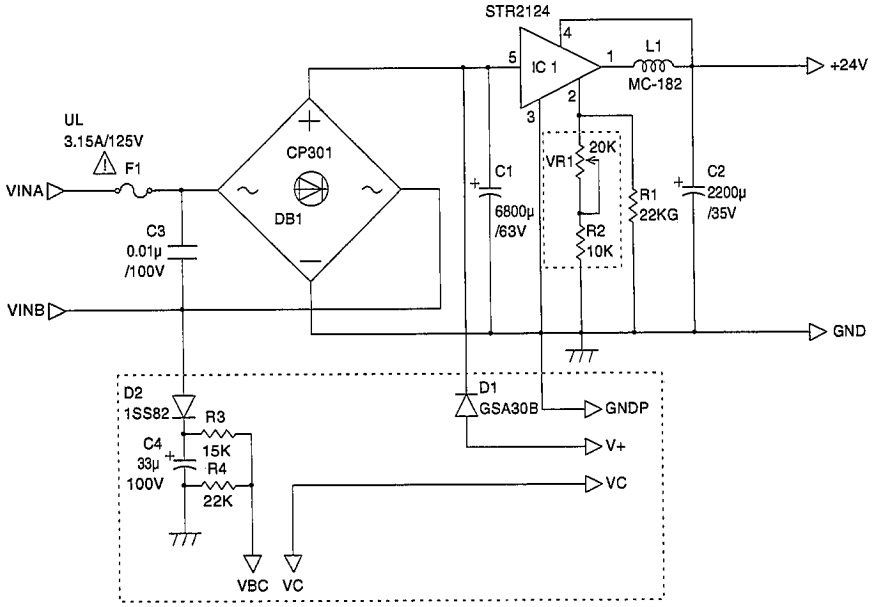
4. RS232 I/F PWB circuit diagram



5. RS232C I/F PWB layout



6. Power supply PWB circuit diagram



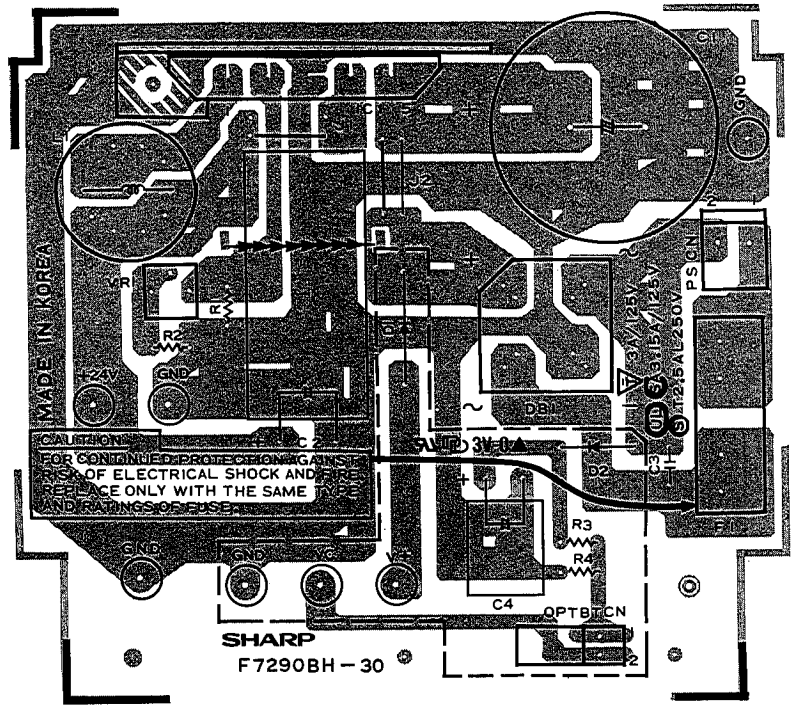
VIN CN

PIN	SIGNAL
1	VINA
2	VINB

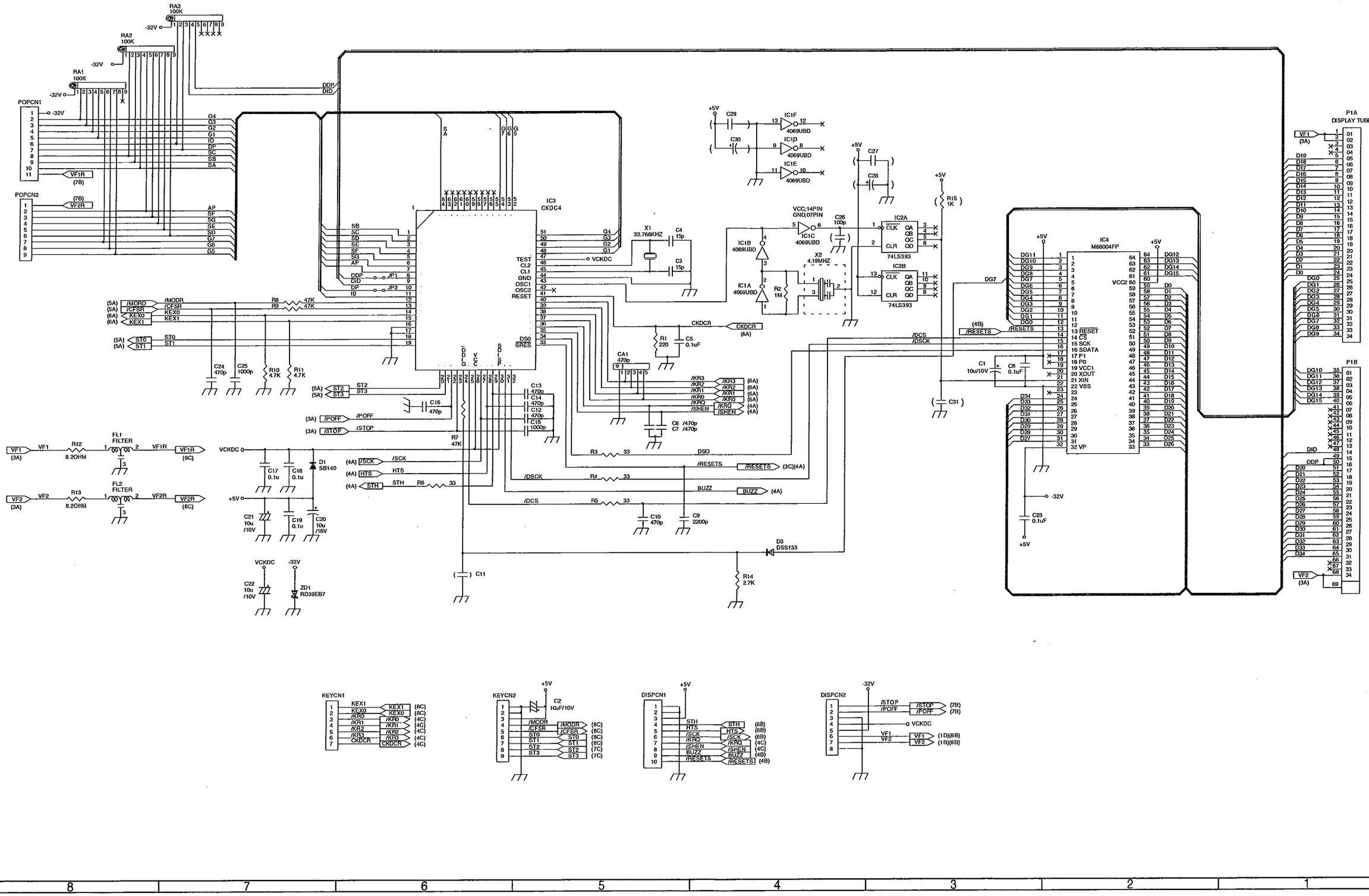
PIN	SIGNAL
1	V+
2	VC
3	GND

PIN	SIGNAL
1	VBC
2	VC

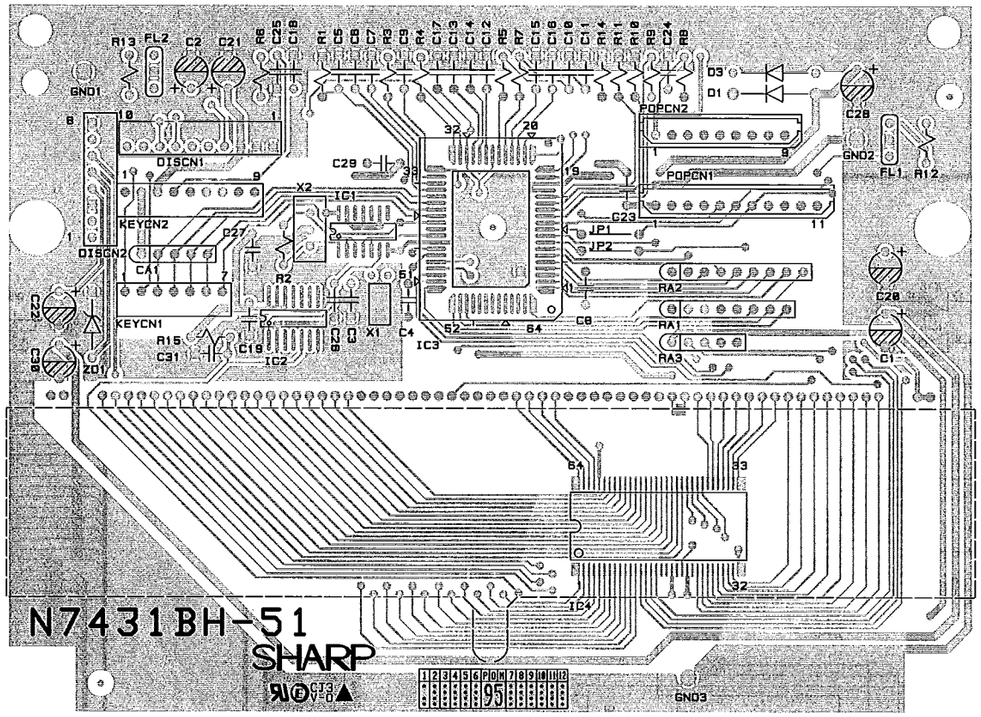
7. Power supply PWB layout



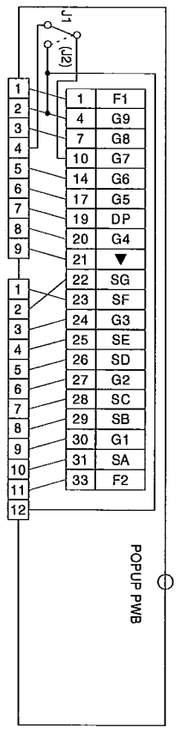
8. Display PWB circuit diagram



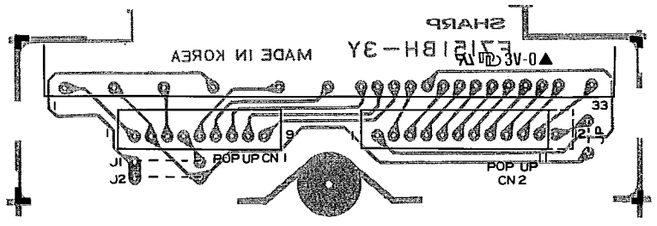
9. Display PWB layout



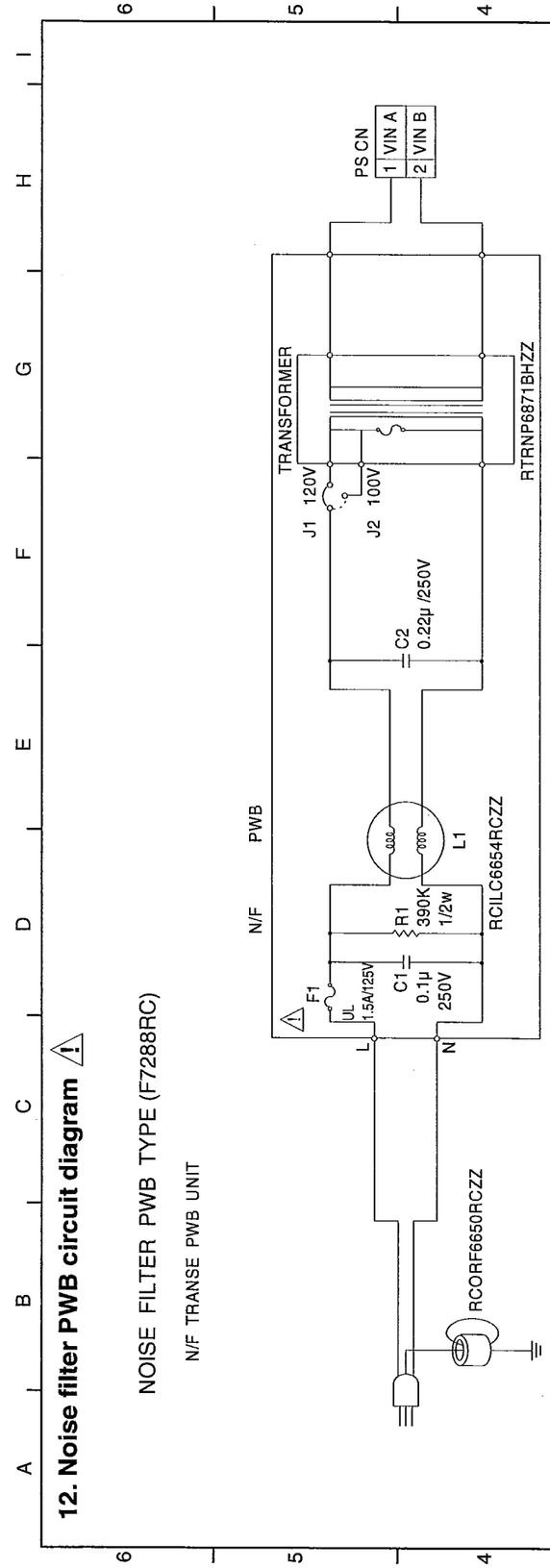
10. Pop-up display PWB circuit diagram



11. Pop-up display PWB layout



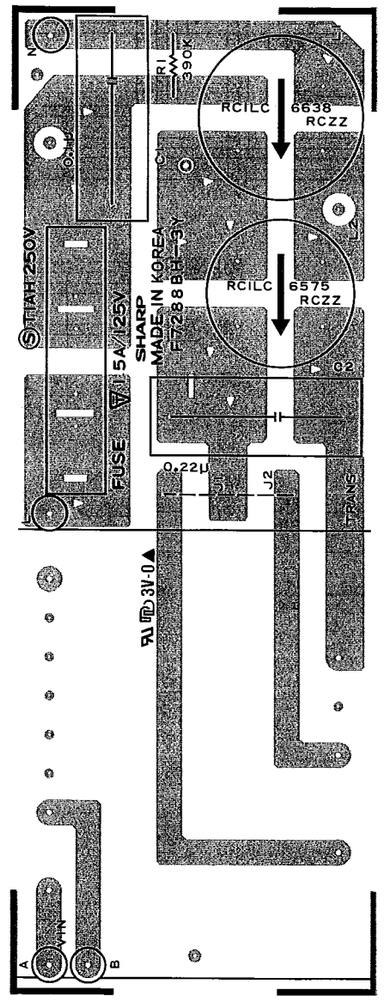
12. Noise filter PWB circuit diagram



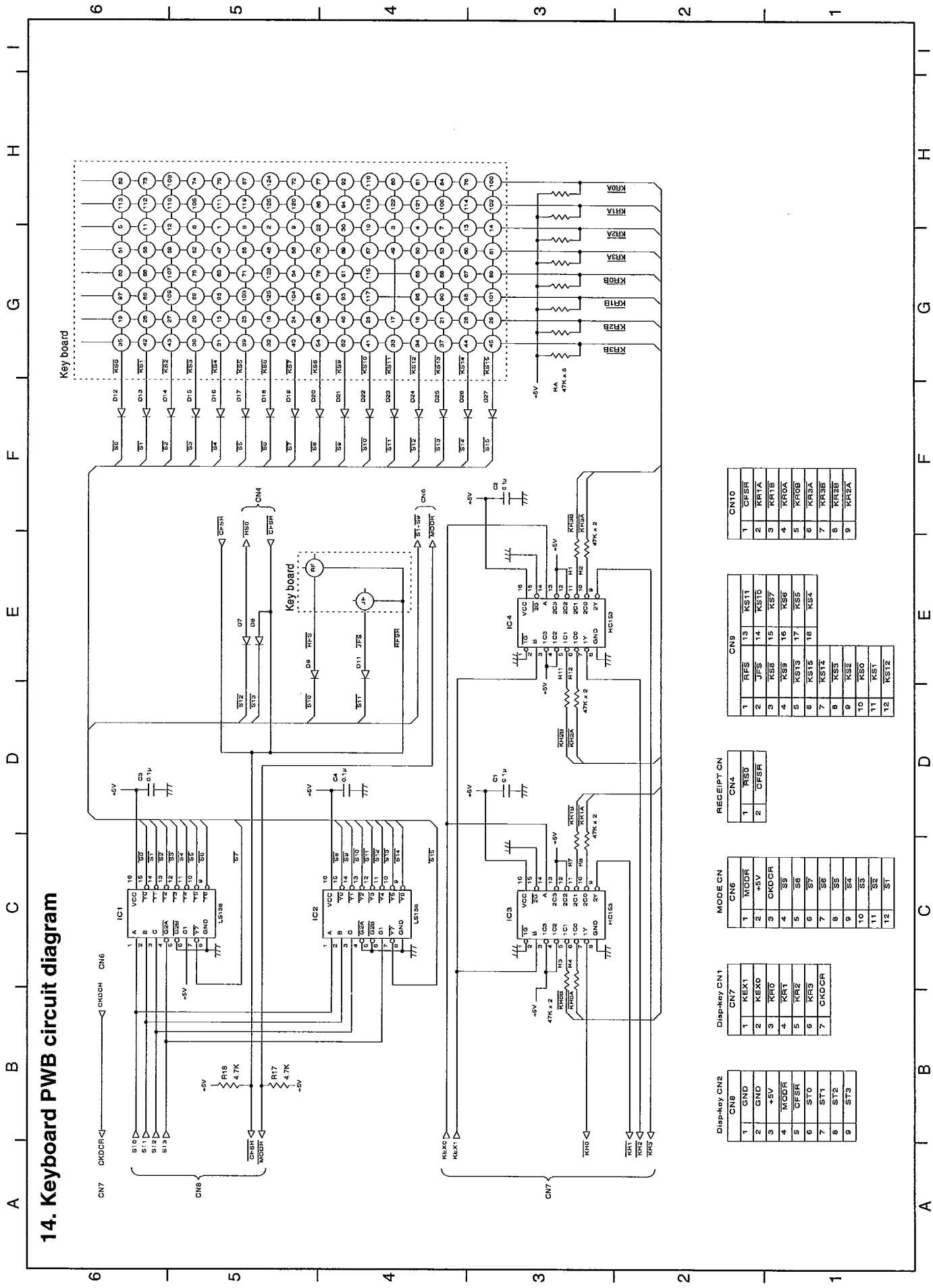
NOISE FILTER PWB TYPE (F7288RC)

N/F TRANSE PWB UNIT

13. Noise filter PWB layout



14. Keyboard PWB circuit diagram



15. Keyboard position code table

↑ RECEIPT	↑ JOUNAL	22	30	38	46	54	62	70	78	86	94	102	110	118	126
7	14	21	29	37	45	53	61	69	77	85	93	101	109	117	125
6	13	20	28	36	44	52	60	68	76	84	92	100	108	116	124
5	12	19	27	35	43	51	59	67	75	83	91	99	107	115	123
4	11	18	26	34	42	50	58	66	74	82	90	98	106	114	122
3	10	17	25	33	41	49	57	65	73	81	89	97	105	113	121
2	9	16	24	32	40	48	56	64	72	80	88	96	104	112	120
1	8	15	23	31	39	47	55	63	71	79	87	95	103	111	119

SHARP

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